Проведено аналіз складних структур різної архітектури ІС/БІС на епі-шарах GaAs, сформованих на Si-підкладках. Виявлено вплив процесів розсіюваних носіїв заряду на флуктуаціях потенціалу на величину і профіль рухливості електронів по товщині епітаксіальної структури. Експериментально показано, що підвищення крутизни в транзисторах Шотткі на основі структур із заглибленими шарами можливе при зниженні опору паразитних областей затвор-стік, затвор витік

Ключові слова: комплементарні структури, напівпровідники, епітаксія, інтегральні схеми, технологічні особливості

Проведен анализ сложных структур различной архитектуры ИС/БИС на эпи-слоях GaAs, сформированных на Si-подложках. Выяснено влияние процессов рассеивания носителей заряда на флуктуациях потенциала на величину и профиль подвижности электронов по толщине эпитаксиальной структуры. Экспериментально показано, что повышение крутизны в транзисторах Шоттки на основе структур с углубленными слоями возможно при снижении сопротивления паразитных областей затвор-сток, затвор-исток

Ключевые слова: комплементарные структуры, полупроводники, эпитаксия, интегральные схемы, технологические особенности

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RESEARCH INTO CONSTRUCTIVE AND TECHNOLOGICAL FEATURES OF EPITAXIAL GALLIUM-ARSENIDE STRUCTURES FORMATION ON SILICON SUBSTRATES

S. Novosyadlyj
Doctor of technical sciences, Professor*
E-mail: nsp@pu.if.ua
B. Dzundza
PhD*
E-mail: bohdan.dzundza@pu.if.ua
V. Gryga
PhD, Associate Professor*
E-mail: v.dr_2000@ukr.net
S. Novosyadlyj
Lead Engineer
Soft Serve
Sakharova str., 23, Ivano-Frankivsk, Ukraine, 76000
E-mail: gr@softserveinc.com
M. Kotyk
Postgraduate student*
E-mail: mishanyakit@gmail.com
V. Mandzyuk
Associate Professor*
E-mail: mandzyuk_vova@ukr.net
*Department of computer engineering and electronics
Vasyl Stefanyk Precarpathian National University
Shevchenko str., 57, Ivano-Frankivsk, Ukraine, 76018

1. Introduction

The progress in the development of IC/LSI technologies on GaAs was characterized by significantly worse success than provided previously [1–3]. In particular, this is due to the problems of obtaining reproducible, less-defective initial materials and structures on Schottky field transistors (ShFTs) of submicron size with a small dispersion of the output parameters over the substrate plane.

Development of the technology for obtaining reproducible, less-defective epitaxial gallium-arsenide structures of ShFT and non-destructive methods of electrophysical test control of the conductivity and mobility of electrons in GaAs epitaxial structures remains relevant and allows improving significantly the characteristics of LSI in general.

2. Literary review and problem statement

Silicon has always played a decisive role in the technology of integrated circuits as the main semiconductor material. In recent years, semiconductor compounds as $A^{III}B^{V}$ (for example, GaAs) have been used as an alternative. Since 2010, the volume of commercial products based on gallium arsenide has increased by several times [4]. This growth trend persists until now. One of the applications of GaAs electronic devices is microwave electronics. Typical values of the diameters of grown ingots are 100–150 mm, and commercial crystals of 200 mm in diameter have appeared [5].

The dielectric layers of Al_2O_3 are promising for GaAs structures. The main method of their obtaining at present is the atomic layer deposition method [6, 7]. Certain success

has been achieved with the creation of a field GaAs transistor based on Al_2O_3 MOS-structures [7].

Decreasing of geometric sizes of transistors results in decreasing the crystal area, parasitic capacitances, LSI energy consumption and increasing the speed. In recent years, the gate length of the MOS-transistor has decreased to less than 60 nm [8]. Today, special attention is focused on the architecture of structures for the LSI at submicron range [9, 10]. It is the architecture that qualitatively expresses the question of technology: the growth of structures, the formation of functional layers and circuitry [11, 12].

The technology of obtaining of high-purity GaAs crystals is quite expensive, so there is a necessity in the development of epitaxial technologies for the formation of GaAs structures on Si-substrates, which are currently not sufficiently investigated. These technologies, combined with non-destructive methods of electrophysical diagnostics of reliability at the stage of manufacturing the crystal, can significantly reduce the cost of LSI manufacturing.

3. The aim and objectives of the study

The aim of the work is to develop submicron technology for obtaining less-defective epitaxial gallium-arsenide structures on Schottky transistors on silicon substrates using test diagnostic control. This will increase the speed of the LSI and reduce their production costs.

To achieve this goal, the following tasks were performed:

– technology of forming and designing of complementary pairs of ShFTs on GaAs epitaxial layers is developed;

– test elements (hallotrons) are developed for technological control of parameters (mobility of charge carriers) of ShFTs;

– design technological analysis of complex structures of LSI circuits on GaAs epitaxial layers with the use of high-speed complementary ShFTs is carried out.

4. Influence of architecture on the ShFT parameters

As it was previously established, the movement of the ShFT channel both to the free surface of the epitaxial layer and to the interface of the active layer/substrate causes a marked decrease in steepness [13, 14]. As the profile measurements of drift mobility shown (Fig. 1), the processes of electron scattering have a significant influence on the imperfections of the specified boundaries of the structure. Therefore, it is important to construct such architecture for the IC/LIC, in which the ShFT channel is equidistant both from the input surface and from the substrate. The transition to the Si-substrate increases not only the heat transfer, but also allows the use of a large diameter of the substrate (>150 nm) with the use of automated systems of structured processing of plates of silicon technology. Here, the development option is δ-structures and heterostructures for transistors with a high mobility of electrons (7500 $cm^2/V{\cdot}s$) at 300 K, and larger than 10^5 cm^2/V s at 77 K. However, the significant complication of the growth technology of heterostructures and manufacturing on their basis of high-speed IC/LIC, as well as low current density in the channel (in the 2D-region) somewhat restrain widespread use of the elemental base on GaAs-architectures.

The prospect of δ-structure using at elevated temperatures (>300 °C) is due to high values of the solubility of doping impurities ($N=5{\cdot}10^{13}$ cm^{-2}), which significantly increases the specific conductivity, despite the low mobility (μ=2000–3500 $cm^2/V{\cdot}s$) under conditions of strong doping. As a result, there is a potential possibility to increase the ShFT steepness by reducing the distance between the δ-layer and the gate metal, as well as by reducing specific resistance of the parasitic areas of source and drain.

As parameters that accurately determine the characteristics of ShFTs and the speed of the IC/LIC, we used: the mobility of charge carriers and the conductivity of the epitaxial structures, specific resistance of the source-drain contacts of ShFTs, the saturation current and the specific steepness of ShFTs, as well as the dispersion along the substrate-plate of large diameters (>150 nm) of the above parameters of test transistors, which determine the yield of suitable structures. The conductivity and mobility of electrons in GaAs epitaxial structures were measured by non-destructive methods of electrophysical test control for the diagnosis of LSI structures. To measure mobility, test structures, called hallotrons, were developed [15]. Here the non-destructive low-signal, magnetoresistive, Hall, volt-farad and volt-ampere characteristics are used in full.

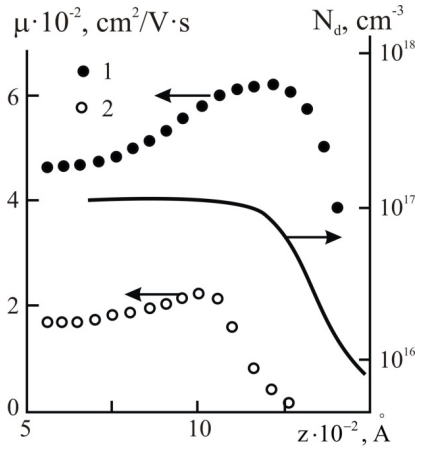

Fig. 1. Profiles of mobility and concentration of electrons for structures with homogeneous doping for GaAs-layers at different temperatures: 1 — 77 K; 2 — 300 K

In structures with deepened donor layers (δ-layers) there is no significant difference in the dependence of mobility on the thickness of depth of the donor layer up to a thickness of about 80 Å (Fig. 2, *a*). On the contrary, dependence of the mobility on the product of concentration and thickness of the epitaxial layer (Fig. 2, *b*) is significant and, taking into account data (Fig. 2, *a*), is explained by the factor of scattering of charge carriers at the donor impurity of doping.

Here, the optimum depth of the donor layer is 550±50 Å, as the decrease in depth leads to a decrease in the mobility of electrons in the structure, and an increase – to the growth of resistance of parasitic source-drain regions. There is a sharp decrease in the electron mobility precisely in structures with deepened donor layers, starting with a distance of 250–270 Å. This is most likely due to the influence of the fluctuations in the potential of the nascent centres of donor layer (n-GaAs). This is confirmed by the decrease in the absolute value of mobility for deepened layers with a thickness less than 50 Å, an increase in the temperature, at which significant scattering on phonons occurs, and an increase in the dispersion of local conductivity in area of the

plate-substrate. The fluctuations of thickness of the auxiliary layer give also a certain contribution to the growth of the conductivity dispersion.

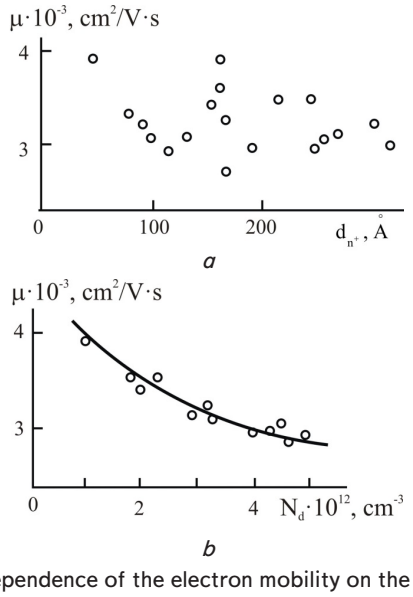

Fig. 2. Dependence of the electron mobility on the thickness of deepened layer (a) and the product of concentration on the thickness of the deepened layer (b) for GaAs epitaxial layers

To reduce the thickness of the donor layer (up to the values of one monolayer <5–10 nm) without worsening the dispersion of local conductivity in the area of the substrate, it was possible to use gas-phase epitaxy from metalorganic compounds (MOC): trimethylgallium $Ga(CH_3)_3$ or triethylgallium $Ga(C_2H_5)_3$, and trimethylarsenic $As(CH_3)_3$. In this case, the best homogeneity of local conductivity in the area of substrates ($\Delta\sigma/\sigma \leq 0.02$) is reached in the doping range of donor admixture of 10^{11}–$5 \cdot 10^{17}$ cm^{-3} (Table 1). However, there is a significant decrease in integral mobility for δ-layers (Table 1), and the profile measurements have shown that a sharp decrease in mobility cannot be avoided within the 250±50 Å δ-layer (Fig. 3).

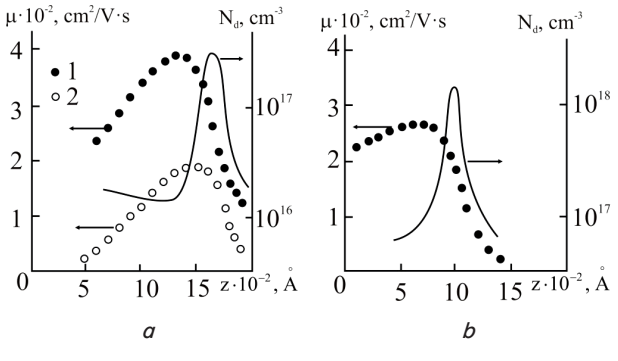

Fig. 3. Profile of mobility and concentration of electrons at different temperatures (1—77 K, 2-300 K): *a* — structures with deepened n-GaAs-layer; *b* — structures with δ-layer

The reason for the sharp decrease in mobility in δ-structures is, most probably, also due to the scattering of electrons on a charged donor impurity and on potential fluctuations near the charged plane of the δ-layer. This is indicated by the monotonous drop in mobility when moving from the δ-layer to the substrate side.

The influence of conductivity heterogeneity of the initial GaAs epitaxial structures on the dispersion of the output parameters of ShFTs was studied on experimental test structures both at the stages of interoperational control and during their formation. This allowed us to thoroughly investigate the effect of specific technological operations on the magnitude of the output parameters of ShFTs and their dispersion. Such ShFTs had the following parameters: channel length – 0.6 μm, gate length – 2 μm, channel widths – 24 and 10 μm. Moreover, complementary ShFTs were formed, on which CMOS-circuits can be formed. All data are summarized in Table 1.

As can be seen from Table 1, transition from homogeneously doped GaAs epitaxial layers to δ-doped layers is characterized by an increase in the steepness S of ShFTs and a significant decrease in the parasitic resistance R_s of the drain-source regions. The increase of steepness S occurs in spite of a certain decrease in the mobility of electrons in the original structures. This is due to the reduction of the distance between the gate and the channel and the reduction in the resistance of the parasitic drain-source regions, as well as due to the increased conductivity.

An analysis of the effect of various processes for the production of ShFT-structures showed that the most significant dispersion is made by the processes of Shottky gate forming, which include the plasmachemical etching of surface layer and the deposition of the metal. The comparison of homogeneous and δ-doped structures shows that the dispersion of steepness and saturation current of ShFTs on structures with complex profile does not decrease, despite the increase of uniformity of structures. This is due to the close placement of the channel to the metal-semiconductor interface, which is weakly controlled in the process of forming the ShFTs. In other words, the implementation of devices with higher parameters in the δ-structures requires a corresponding change in the technology of ShFT formation, namely the use of multi-charge ion implantation. Thus, the further growth of steepness S is impossible without significantly reducing the resistance of the drain-source regions. This, in turn, requires the use of retrograde construction of ShFTs, in which the length of the channel and the gate coincide. A reduction of dispersion on the substrate can be easily achieved by combining surface preparation, etching, metal deposition, its ionic milling, or using sharp p-n-junctions instead of Schottky gates. For the formation of complex ShFT profiles, the original technological processes are used:

– low-temperature epitaxy based on MOCs and microwaves;

– formation of a buffer layer of germanium for the equating of crystalline lattice constants of silicon and gallium arsenide;

– multi-charge ion implantation for the formation of retrograde drain-source regions with low resistance;

– formation of a tungsten nitride gate (WN_x);

– formation interlayer (Cr^{++}) and local isolation (B^{++}, O^{++}, H^{++}) by multi-charge implantation using diffusion processes;

– deposition of capsular coatings of AlN or Si_3N_4 by high-frequency magnetron sputtering of Al- or Si-targets;

– precision lithography and ionic milling of the AuGe-12 alloy;

– anisotropic plasmachemical ettching and the use of getter technology.

Table 1

Electrophysical parameters of ShFTs on GaAs epitaxial structures

No.	Architecture of GaAs epitaxial structure	Electrophysical parameters								
		$\sigma\cdot10^{-3}$, Sm/mm	D_σ	μ, $cm^2/V\cdot s$	I_s, mA/mm	D_{IS}	S, mA/V mm	D_s	R_s, Ohm·mm	D_{Rs}
1	Homogeneous doping: 0.18 μm, $1.1\cdot10^{17}cm^{-3}$	0.71	0.18	4500	40	0.39	50	0.25	5.0	0.18
2	Homogeneous doping: 0.25 μm, $1.7\cdot10^{17}$ cm^{-3}	0.66	0.07	3500	60	0.25	70	0.15	2.0	0.15
3	Deepened n-GaAs-epitaxial-layer: 0.01 μm, $1\cdot10^{18}$ cm^{-3}	0.51	0.06	3100	57	0.18	64	0.22	2.5	0.12
4	δ-layer: $7\cdot10^{12}$ cm^{-3}	3.9	0.04	2700	45	0.20	92	0.23	0.8	0.10

Note for parameters: σ – conductivity of the output structures; μ – Hall mobility of electrons; I_s – saturation current; S – steepness; R_s – resistance of the drain-source regions; D_σ, D_{IS}, D_s, D_{Rs} – variance of parameters

It should be noted also that the possibility of obtaining strongly-doped δ-layers with N=(1–5) 10^{12} cm^{-2} also allowed them to be used as contact δ-layers in the structures of IC/LSI (specific resistance of the system AuGe-12/contact δn^+-layer GaAs is less than 0.2 Ohm mm). This is especially important in the development of IC/LSI on the basis of self-aligned technology and reproduces the possibility of using tunnel contact systems for drain-source regions. Such systems have an order of magnitude better morphology compared to the traditional technology of forming contacts.

5. GaAs based hallothrons as test elements for measuring the mobility of charge carriers-LSI speed

Two types of hallotrons (I and II) were studied on the basis of the epitaxial n-GaAs and GaAs structures, which differ in the material of semi-insulating substrates from monocrystalline GaAs. The substrates of semi-insulating GaAs doped by chromium (Cr) (for variant I) and semi-insulating GaAs doped by indium (In) (for the variant II) were used. Parameters of semi-insulating materials are given in Table 2.

Table 2

Electrophysical parameters of substrates for hallotrons

No.	Kind	Orientation	Resistivity ρ, Ohm·m	Density of dispersion N_D, cm^{-2}
1	I	(100)	10^8	$1.5\cdot10^4$
2	II	(100)	10^7	$9\cdot10^9$

The active layers of the test structure were obtained by the method of gas-phase epitaxy on a horizontal type device "Isotrop 3" on the substrates of both types with a diameter of 35±5 mm. The concentration of free electrons is n=$1.5\cdot10^{16}$ cm^{-3} and the mobility of charge carriers is μ=(4500–6000) $cm^2/V\cdot s$ in undoped epitaxial films of n-type conductivity of 3.5 μm in the thickness. The instrument test structure – the hallotron was made in the form of a symmetrical cross with the size of the active region on the width of the scribing band (Fig. 4). The technology of its formation is given in [16, 17]. The physical vapour deposition of contact pads is carried out through a mask with a pre-deposited pyrolysis method of SiO_2 (Si_3N_4) layer with lithograph windows created. Au-In-Ge system was used for high-quality ohmic contacts. The firing of contacts was carried out in a medium of form-gas (N_2–H_2) at t≤575 °C for 5 min. Then the mesostructure underwent etching. The effect of semi-insulating substrates GaAs on electrophysical parameters of test structures were shown on the example of formation of hallotrons of type I and II with sensitivity γ=100 V/A·T. Their sensitivity was determined at a control current I=5 mA in a magnetic field with an induction B=0.5 T. These are the test elements for determining the mobility of carrier carriers as the main parameter of high-speed arsenide-based LSI.

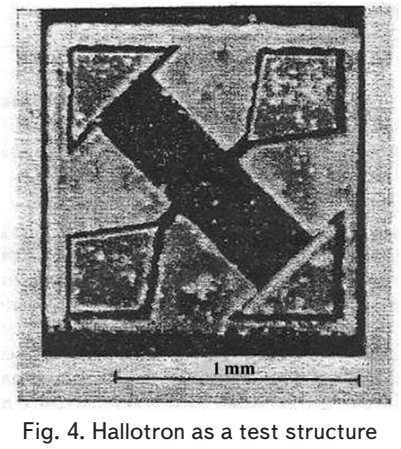

Fig. 4. Hallotron as a test structure

Fig. 5 shows dependences of Hall voltage V_x and resistance R as function of magnetic induction for three values of the control current for hallotrons of type I and II. The magnetic induction was measured in the range from 0 to 1 T using the digital teslameter "Seitron Doaneri" 3102A. Experimental data were obtained at room temperature. Hall voltage V_x was measured using a digital multimeter "Philips PM2528".

The higher linearity of dependence $V_x=\psi(B)$ for the type I hallotron was well observed visually, especially at the control current I=10 mA. At the same time, for type II hallotrons, there is an extremely high linearity in the magnetic induction range of 0–0.3 T.

The nonlinearity of dependence $V_x=\psi(B)$ can be quantified for different magnetic field induction ranges using formula:

$$\phi = \frac{v_x = \psi(B)/B}{v_x = (0,1)/0,1} \cdot 100\,\%. \quad (1)$$

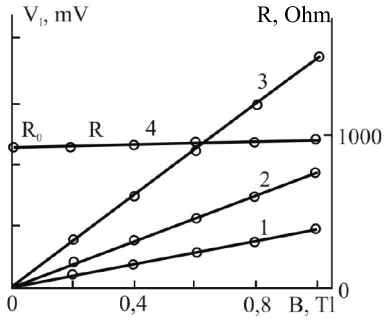

Fig. 5. The Hall voltage for three values of the control current (2.5, 5, and 10 mA – curves 1, 2, 3, respectively) and resistance (curve 4) as a function of magnetic induction

The resistances of these hallotrons vary with the change in magnetic induction in accordance with expression $R_0(1+MB^2)$, that causes the magnetoresistance effect. The magnetoresistive coefficient is $M=0.28\ T^{-2}$ for type I hallotrons, and is $0.058\ T^{-2}$ for type II.

Values of the non-linearity for the type I and II hallotrons, calculated using the above formula, for two values of magnetic induction at the control current I=5 mA are given in Table 3.

Table 3

Electrophysical parameters of hallotrons formation

		I	II
ψ, %	B=0.5 T	4.0	0.8
	B=1 T	13.3	1.2

Temperature stability is one of the most important characteristics of the hallotron. The dependence of Hall voltage on control current and temperature dependence Hall voltage and resistance of devices for two types of hallotrons are shown in Fig. 6, 7, respectively. The investigation was realised in the temperature range from –200 to +200 °C.

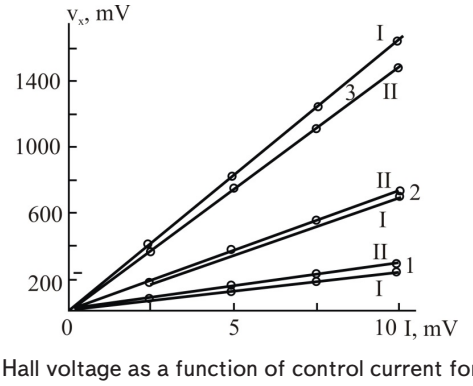

Fig. 6. Hall voltage as a function of control current for both I and II types of hallotrons

Temperature dependences of Hall voltage were measured using a cryostat-table placed in a magnetic field B=0.5 T at I=2 mA to prevent heating. Here V_x smoothly decreases with temperature in this temperature range. In this case, the thermostability of the II type hallotron is better at high temperatures – the temperature coefficient is almost an order of magnitude smaller at T=+150 °C.

The temperature coefficients (TC) of Hall voltage are calculated for three temperatures and have the following values for both types (I, II) of the hallotrons (Table 4).

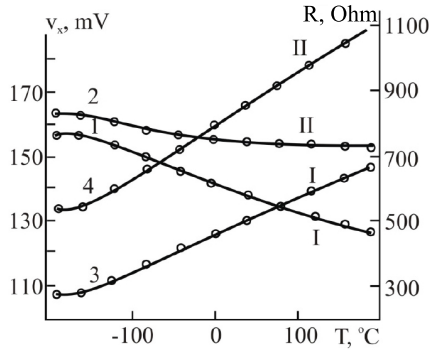

Fig. 7. Temperature dependences of Hall voltage (1, 2) and resistance (3, 4) for both I and II types of hallotrons

Table 4

Temperature coefficients of Hall voltage

Type	TC V_x, K^{-1}		
	–50 °C	+20 °C	+150 °C
I	$6.8\cdot10^{-4}$	$5.4\cdot10^{-4}$	$5.8\cdot10^{-4}$
II	$3.2\cdot10^{-4}$	$1.1\cdot10^{-4}$	$8.7\cdot10^{-4}$

The temperature dependences of resistances are practically linear in the range from –160 to +190 °C and from –140 to +190 °C for I and II type hallotrons, respectively. The temperature coefficients of resistance for I and II type hallotrons are close to the values of $2.4\cdot10^{-3}$ and $2.2\cdot10^{-3}\ K^{-3}$, respectively. In general, the hallotrons on GaAs<In> substrates have lower values V_x compared to ones for hallotrons on traditional GaAs<Cr> substrates.

6. Discussion of results: complementary Schottky field transistors as elements of LSI on GaAs heterojunction

A promising element of digital high-speed IC/LSI and analog microwave chips of the microwave range is a heterostructured field-effect transistor with a control transition – a metal-semiconductor (Me-S). In this transistor, the properties of the heterojunction between thin monocrystalline layers (δ-layers) of both semiconductor materials with close parameters of crystalline lattices, but different width of the band gap, are used. The most commonly used is the heterojunction between gallium arsenide (GaAs) and gallium-aluminum-arsenide ($Al_xGa_{1-x}As$) (Fig. 8). The x value indicates the relative content of Al. The width of the band gap ΔE of gallium-aluminum-arsenide ($Al_xGa_{1-x}As$) linearly increases with x. For typical value x=0.3 ΔE=1.8 eV.

The equilibrium energy diagram of the heterojunction between undoped GaAs and doped by donor impurities (for example, Si) gallium-aluminum-arsenide, is given in Fig. 8. The Fermi level E_F is given dashed horizontal lines (its energy is identical for both types of x in equilibrium state); E_v is the energy of the boundary of the valence band; E_c is the boundary of the conduction band. The Fermi level is located almost on the boundary of the conduction band for undoped GaAs (1), and in the donor-doped $Al_xGa_{1-x}As$ (2) with $N_D=(1–20)\ 10^{17}\ cm^{-3}$ close to E_c.

In GaAs near the interface 5 of two semiconductors in the conduction band, region 3 with minimum electron energy is formed. In this region, the accumulation of electrons takes place, which pass from region 4, located in $Al_xGa_{1-x}As$.

Region 4 is depleted by electrons and is positively charged (+), since it contains non-compensated donor ions. The energy jump ΔE_n for the conduction band is about 0.3 eV at the interface 5 at x=0.3.

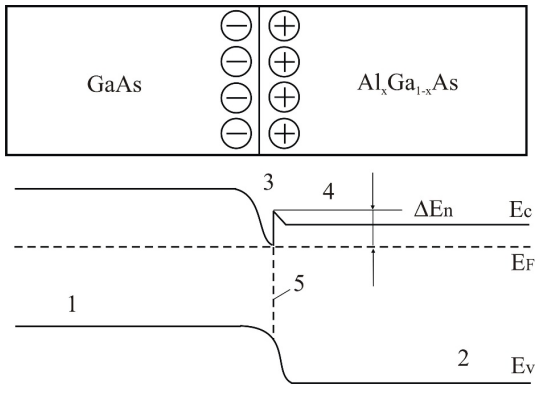

Fig. 8. Energy diagram of the GaAs-Al_xGa_{1-x} as a heterojunction

The electrons, accumulated in region 3, are located in a potential well and can move in weak electric fields only along the interface 5 in the plane perpendicular to the plane of Fig. 8. Therefore, such a set of electrons in the region 3 is called a two-dimensional electron gas (2DEG), thus emphasizing that in the weak fields these electrons cannot move in the third dimension.

The electrons that formed the 2DEG arise due to the thermal ionization of the donor levels in AlGaAs, where the impurity concentration is large ($>10^{17}$ cm^{-3}), and moves to the region 3, located in the undoped GaAs, where the impurity concentration is small ($<10^{14}$ cm^{-3}). Thus, one achieves the spatial separation of free electrons (in region 3) and scattering centers (acceptor ions), concentrated in $Al_xGa_{1-x}As$.

Rather low surface state density and defects at the interface are provided in the heterojunction due to the corresponding achievement of the crystalline lattice parameters of these two semiconductor materials. For these reasons, for electrons, accumulated in region 3, very high mobility is achieved in weak electric fields, which is close to bulk mobility for undoped GaAs $(8–10)\cdot10^{-3}$ $cm^2/V\cdot s$ at T=300 K. Since the lattice scattering predominates in the non-dopeg GaAs layer, electron mobility increases sharply with a temperature drop to 77 K. For better spatial separation of 2DEG and scattering centres between undoped GaAs and donor-doped $Al_xGa_{1-x}As$, a thin (δ-layer of several nanometers in thickness) separating (buffer) layer of undoped $Al_xGa_{1-x}As$ is formed. The concentration of scattering centres in the separating undoped layer is lower than in the doped that, therefore, the mobility of the electrons, accumulated in region 3, is increased additionally on 10–20 %. Temperature dependence of electron mobility for 2DEG in heterostructure with δ-separating layer is shown in Fig. 9, *a* (curve 1). The mobility of electrons increases to $1.4\cdot10^5$ and $2\cdot10^6$ $cm^2/V\cdot s$ at a temperature of liquid nitrogen (77 K) and liquid helium (4 K), respectively. The temperature dependence of electrons in GaAs layer containing a donor with a concentration of 10^{17} cm^{-3} is given in the Figure (curve 2).

The mobility of electrons in 2DEG, especially at low temperatures, depends strongly on the technology of δ-layers formation. Different methods of epitaxial growth of thin semiconductor layers are used for their formation. The best quality of the epitaxial layers in the heterostructure is achieved by MOC- and microwave epitaxy.

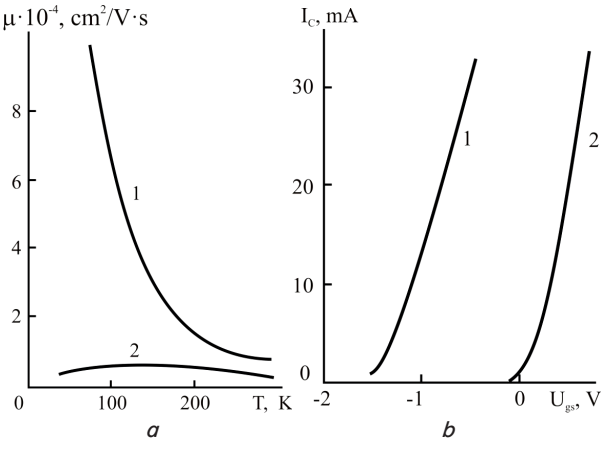

Fig. 9. Temperature dependence of electron mobility for 2DEG-layer (*a*) and drain-gate characteristics of ShFT (*b*): normally open (1) and normally closed (2)

The above-described heterojunctions are used in structures of high-speed field transistors with a controlled the Me-S transition. Such example of the design execution of a normally open and normally closed ShFT is shown in Fig. 9. In the manufacture of normally open ShFTs on chromium-doped semi-insulating substrates with GaAs, the MOC-epitaxy forms sequentially: undoped GaAs layer of p-type conductivity, undoped separating $Al_xGa_{1-x}As$ layer, silicon-doped ($N_D=7\cdot10^{17}$ cm^{-3}) gallium-aluminum-arsenide layer. WN_x is used for the formation of the gate 3, and AuGe-Ni alloy – for contacts of drain-source regions. In normally closed ShFT with an induced canal, the upper layer of gallium-aluminum-arsenide is partially etched to a thickness of 50 nm. In this way, normally open and normally closed ShFTs are manufactured on one substrate. Threshold voltage of such ShFTs is determined by expression:

$$U_T = \varphi_{0n} - \frac{\Delta E_n}{q} - \frac{qN_D d^2}{2\varepsilon_0\varepsilon_{nz}}, \qquad (2)$$

where φ_{0n} is the equilibrium height of the potential barrier of Me-S transition; d is the total thickness of donor-doped and undoped layer (δ-layer) of gallium-aluminum-arsenide ($Al_xGa_{1-x}As$); ε_{0n} is its relative dielectric permittivity; ε_{nz} is the dielectric permittivity of charge accumulation region; q is the electron charge.

The principle of the operation of the hetero-MOS transistors (HMOS – ShFTs based on the Me-S barrier) is similar to that of the MOS-transistor. Me-S control transition is formed between the metal gate and the $Al_xGa_{1-x}As$ layer placed below it. The depleted region of this transition is mainly located in gallium-aluminum-arsenide layers.

The channel of normally open transistor is formed at gate-source voltage $U_{gs}<0$ in the layer of undoped GaAs at the boundary with a heterojunction in the accumulation region, where 2DEG is formed. The control gate-source voltage affects a change in the thickness of the depleted region of Me-S transition, the concentration in the accumulation region and the drain current. If negative (modulo) gate-source voltage is sufficiently large (equal to the threshold voltage U_T), the depleted region expands so that it completely

overlaps the accumulation region of electrons. Drain current stops at the same time.

At normally closed ShFT due to the lower thickness d of the upper layer of $Al_xGa_{1-x}As$ layer (at $U_{gs}=0$), the conductive layer is absent, since accumulation region of 2DEG is overlapped by the depleted region of control transition. The channel arises at a certain potential (voltage) equal to the threshold one, so depleted region of the control transition Me-S is so that its lower boundary enters the accumulation region of electrons.

Fig. 9, b shows the drain-gate characteristics of normally open (1) and normally closed (2) ShFT with a gate length $L_g=0.8$ μm and a drain-source distance of 4 μm. Due to the high mobility of electrons and the small length of the gates, the saturation of the drift velocity of the electrons in the channel is achieved practically in the whole range of the gate voltage change, and the linear dependence occurs

$$I_C = S'(U_{gd} - U_T - E_{cr})L_g, \quad (3)$$

where E_{cr} is the critical field strength, $S'=S/(1+R_0S)$ is the steepness characteristics $S=\varepsilon_0\varepsilon_{nz}U_{sat}b/d$; b is the thickness of deepened metal layer.

The value S'/b is 117 and 173 mS/mm for curves 1 and 2, respectively. Greater value of the steepness for normal closed transistor is due to smaller thickness of donor-doped gallium-aluminum-arsenide ($Al_xGa_{1-x}As$).

An important advantage of the ShFT structure o the Me-S barrier (HMOS), compared with the MOS-transistor one, is the lower the density of surface states at the boundary between the gallium-aluminum-arsenide with dielectric and the high value of the Schottky barrier ($\varphi_{OC}\cong 1$ V). The negative surface charge and the thickness of the depleted regions in the interval of source-gate and gate-drain are reduced due to the lower density of surface states. It results in smaller parasitic resistance of these areas without the use of additional technological operations of ion doping that are necessary for transistors with self-aligned gate.

The pulse and frequency properties of ShFT are mainly determined by the transit time of electrons t_{tr} through the channel of length L_g, where they move with the saturation speed υ_{sat}: $t_{tr}=L_g/\upsilon_{sat}$. $\upsilon_{sat}=2\cdot10^{17}$ cm/s at T=300 K. The saturation speed increases according to the law $\upsilon_{sat}=1/T$ when the temperature decreases. Such transistors can operate at frequencies up to 150 GHz.

The developed technology of LSI structures formation makes it possible, as a minimum, to reduce by the order the production cost of crystals due to the epitaxial growth of GaAs layers on silicon substrates and the use of technological equipment of silicon technology.

The test element was implemented that allows non-destructive measurement of the mobility of charge carriers in the technological cycle of the formation of LSI structures. The use of epitaxial layers of gallium arsenide eliminates the effects of isoconcentration impurities of oxygen and carbon in gallium arsenide layers that increases their purity.

The research conducted is continuation of long-term experimental work on the formation of sub-and nanomicron LSI structures of high speed [15, 16].

7. Conclusions

1. The technology of formation and construction of complementary structures of ShFT on GaAs epitaxial layers, formed on Si-substrates of large diameter (more than 150 mm), are developed. Its features are the use of silicon technology equipment, as well as sharp decrease in the use of gallium, which reduces the production cost of the crystal.

2. The analysis of engineering and design peculiarities of the formation of epitaxial gallium arsenide structures was carried out, which allowed us to determine the optimal technological conditions for ensuring high mobility of carriers and temperature stability of the characteristics of active elements of the LSI.

3. It is shown that the developed test element – the hallotron allows us to measure the mobility of charge carriers in the technological cycle of the formation of the LSI structures and to realise electrophysical diagnosis of their reliability at the stage of crystal manufacturing.

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