Наведено результати досліджень аналого-цифрового функціонального перетворення із змінною основою логарифму. У відомих аналого-цифрових перетворювачах підвищення швидкодії призводить до погіршення точності і навпаки. На відміну від відомих, розроблений метод дозволяє покращити швидкість перетворення без збільшення похибок. Він реалізується на схемах з комутованими конденсаторами. Оскільки, саме використання явищ перерозподілу та накопичення заряду в конденсаторних комірках дозволяє створити перетворювачі із змінною основою логарифму.

Додатковою перевагою такої реалізації є надійність, мале споживання енергії та висока технологічність виготовлення. Це дозволяє інтегрувати перетворювачі із змінною основою логарифму до різних пристроїв автоматики. Наприклад, як до блоків обчислювачів стаціонарних інформаційно-вимірювальних систем, так і до мініатюрних чи мобільних давачів стану об`єкту.

У ході досліджень розроблено три алгоритми зміни основи логарифма співвідношенням ємностей коденсаторів. Висота кроку перетворення залежить від основи логарифма і змінюється на кожному піддіапазоні перетворення. Спадна розгортка відбувається кроками згори донизу. Вона доцільна для великих вхідних сигналів. Зростаюча розгортка – кроками знизу догори краща, якщо вхідні значення малі. Двостороння розгортка універсальна.

Проведені дослідження дозволили оцінити похибки та час перетворення запропонованого пристрою. Вибрано оптимальну кількість кроків – дозувань на кожному піддіапазоні 10, а також оптимальну кількість піддіапазонів перетворення 4. Для цих значень отримано похибку меншу 0,005 % за час перетворення 100 мкс (40 періодів тактових імпульсів).

Отримані результати дозволяють виготовляти аналого-цифрові функціональні перетворювачі з підвищеними точністю та швидкодією. Вони відповідають кращим світовим аналогам і можуть застосовуватися для різних промислових та наукових задач. Особливістю є можливість задання користувачем як бажаної точності, так і необхідної швидкодії, ще до початку перетворення

Ключові слова: точність, швидкодія, алгоритм, змінна основа логарифму, аналого-цифрове функціональне перетворення, комутовані конденсатори

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DEVELOPMENT OF ALGORITHMS FOR IMPROVING THE ACCURACY AND PERFORMANCE SPEED OF A FUNCTIONAL ANALOG-TO-DIGITAL CONVERTER

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1. Introduction

Accuracy and speed of receiving information from an object is one of the key requirements for ensuring correct operation of the entire automation system. The numbers of sensors and input signals vary. For example, one sensor is required to control the filling of a car tank. It has one input value. Dozens of sensors are used for the control system in a "smart house". Each of them has 1 to 3 input values. The number of sensors in a typical automated line of the food industry exceeds 200. Such numbers are determined by many factors subject to control. In the means and systems of medical, military, and scientific research fields, the number of sensors can be even greater.

To improve technical and operational characteristics of these systems, it is necessary to improve metrological characteristics of the main units, for example, analog-to-digital converters (ADCs) because they provide connection of present-day digital systems with sensors most of which generate analog signals.

At the same time, along with analogue-to-digital conversion, a task of ensuring simultaneous processing of a multitude of input signals and the possibility of functional conversion becomes of special importance.

All these tasks can be performed by functional analog-to-digital converters (FADC) based on switched capacitors.

Most functional analogue-to-digital converters manufactured by leading companies have the following limitations. The number of input signals is not more than three and execution of one particular task: multiplication or division or an exponential function.

The converters based on switched cells allow up to ten input signals to be processed without degradation of accuracy. They also perform a set of at least four functions.

Further improvement of functional analog-to-digital converters is an important task.

2. Literature review and problem statement

Let us consider known solutions for improving analog-to-digital converters. Typical error values for an ADC are 1.6 % for 6 bits, 0.4 % for 8 bits, and 0.1 % for 10 bits. A

logarithmic analog-to-digital converter (LADC) of progressive approximation is considered in [1]. A cell with switched capacitors is used in its design. Improvement of conversion accuracy was achieved by reducing currents of key leakage. Its disadvantages include large (up to 8 pF) parasitic capacitance of keys that reduces speed and the number of required standards equal to the number of bits. Work [2] describes implementation of a low-power cyclic ADC based on switched capacitors. The structure of capacitors of C-2C type was used. The source code of the converter corresponds to 9 bits. However, the conversion characteristic is not logarithmic but linear that shows a narrower dynamic band of input signals. Design and operation of a logarithmic ADC with a pulsed feedback are described in [3]. Quantization error of this converter does not exceed 0.1 %. The feature and advantage of the device consist in implementation of a condenser cell with one condenser due to a pulse feedback. Its disadvantages include a great conversion time (up to 10 ms). Implementation of an integral 8-bit conveyor LADC on switched capacitors is described in [4]. Input cascade of sampling–storing, polarity switching and amplifiers in ADC bits are based on switching capacitors. The converter is manufactured using a 0.18 μm complementary metal-oxide-semiconductor (CMOS) technology. Its dynamic band of input signals is 80 dB (input signals from 0.4 mV to 1 V, signal-to-noise ratio of 36 dB, area of 0.56 mm^2 and power consumption of 2.54 mW). Its disadvantage is that the input signal band is limited to 1 V. An integral conveyor logarithmic ADC realized by the 0.35 μm CMOS technology is described in [5]. Due to the translinear principle of conversion, a simple design and low power consumption were achieved. Power consumption is 3.3 μW at the clock frequency of 1 kHz, input signal band is from 0.7 nA to 100 nA. An 8-bit source code is used. The use of circuits based on switched capacitors makes it possible to significantly reduce power consumed by devices which is especially important for integral execution. In this way, the 64-channel programmable neurostimulator [6] was built in a form of an integrated circuit. It is used in medicine for treatment and investigation of neurological disorders including Parkinson's disease. The stimulator structure includes circuits based on switched capacitors: logarithmic ADC, filters, amplifiers, 64-channel digital-to-analog converter (DAC). The device is manufactured using a 0.18 μm CMOS technology. It takes up 2.7 mm^2 and consumes 89 μW under a normal operation mode and 271 μW with a 1.8 V power supply. Development and implementation of a miniature LADC is proposed in [7]. This device has a cyclic architecture. Its advantage is low power consumption and use of a sensor characteristic for linearization. However, its error less than 2 % corresponds to 6 bits. Comparison of logarithmic and linear ADCs was made in [8] for biomedical applications where broad band signals take place. It was shown that logarithmic ADCs are better in the region of smaller signals but they have higher absolute error at large amplitudes. Realization of a logarithmic ADC based on a net of logical elements is investigated in [9]. Its accuracy is reduced because of logarithm evolution in logical elements. Authors of work [10] propose a converter with low power consumption based on switched capacitors. Emphasis is given to its manufacturability, compactness, smaller losses, and higher overall performance. Peculiarity of its application is work with high voltages, up to 450 V. A new logarithmic converter is proposed in [11]. The device runs according to a recurrent algorithm to improve accuracy and speed. A method of functional analog-to-digital conversion is proposed in [12]. The method is implemented using switched capacitors. The method increases speed due to the parallel element-by-element addition of codes of logarithm taking cells. Disadvantages of devices [11, 12] can be attributed to a relatively complex technical solution.

Most of the known logarithmic ADCs [1, 4–7] or ADCs based on switched capacitors [9, 10] do not provide errors less than 0.4 % and a further reduction in error values relates to a decrease in speed because of an increase in conversion time to milliseconds or tens millisecond.

3. The aim and objectives of the study

This study objective was to increase accuracy and speed of functional analog-to-digital conversion in converters based on switched capacitors with a variable logarithm base.

To achieve the objective, the following tasks were set:

– to develop algorithms for replacing the logarithm base with a ratio of capacitances of capacitors in the cell;

– to perform analysis of errors and duration of conversion by the developed algorithms;

– to compare the results of modeling the developed algorithms;

– to work out recommendations for the application of developed algorithms of ADC with a variable logarithm base.

4. The study materials and methods

4. 1. The general principles of conversion in the FADC based on switched capacitors

The undoubted advantage of the circuits with switched capacitors consists in the phenomena that occur in them and ensure the process of conversion itself, i.e. redistribution and accumulation of charge, will make it possible to derive any value of the logarithm base.

The characteristic of conversion in the FADC based on switched capacitors is logarithmic. They form steps from the change of voltage on the accumulating capacitor.

The conversion characteristic can be constructed with downward steps forming a descending sweep or with upward steps when sweep is ascending. A two-sided sweep is obtained if the sweep direction alternately changes in certain sub-bands.

The logarithm base is responsible for the height of each individual step and accordingly for the conversion speed.

Circuits with a variable logarithm base make it possible to choose the required accuracy and speed of conversion.

Two ways of changing the logarithm base can be realized: by changing the reference voltage or the ratio of capacitances of the cell capacitors since these values affect the height of the voltage step.

The logarithm base in the converters based on switched capacitors depends on the ratio of capacitances of the accumulating and apportioning capacitors:

$$\zeta = \frac{C_N}{C_D + C_N}, \quad (1)$$

where ζ is the logarithm base; C_D is capacitance of the apportioning condenser; C_N is capacitance of the accumulating capacitor; $C_D << C_N$.

Let us consider how conversion occurs with the change of the logarithm base.

First, divide the conversion band into several sub-bands, for example, *m*-sub-bands, and form the compensating voltage *Uk* in each *i*-th sub-band (U_{k_i}) by the following expression:

$$U_{k_i} = U_{B_i}\zeta^{n_i}, \tag{2}$$

where n_i is the number of apportioning in the *i*-th sub-band; U_B is the initial voltage value in the *i*-th sub-band; ζ_i is the logarithm base in the *i*-th sub-band.

In each sub-band, it is necessary to change compensation voltage from the initial level U_B to the moment of transition through the level of the input signal (the moment of equality is fixed by the comparator). The initial level of voltage U_k in the first sub-band is equal to the reference level, i. e. $U_{B_1} = U_0$.

The number of apportioning in the *i*-th sub-band is proportional to the logarithm of the input voltage U_{IN}

$$n_i = \frac{1}{\log\zeta_i}\log\frac{U_{IN}}{U_{B_i}} \tag{3}$$

and it determines the number of steps of the conversion characteristics in each of the sub-bands.

The logarithm base ζ varies in each sub-band.

The value of the logarithm base for a descending sweep depends on the minimum value of the input voltage. For a descending sweep, it depends on the maximum value of the input voltage. The initial value of the compensating voltage affects the logarithm base for both sweeps. The necessary value ζ is physically realized by a changing the ratio of capacitances.

Individual weight ζ of the sub-band corresponds to each sub-band.

The conversion time can be determined as follows:

$$t_{it} = \sum_{i=1}^{m} n \cdot T, \tag{4}$$

where *T* is the period of repetition of clock pulses.

4. 2. The process of conversion with replacement of the logarithm base with a ratio of capacitances and a one-sided descending sweep

To form a descending sweep, set the initial level of the compensating voltage in the first sub-band equal to the reference level, that is, $U_{B_1} = U_0$. The reference value for the descending sweep will correspond to the maximum possible value of the input voltage.

During conversion of the first sub-band, change the compensating voltage U_k from the initial level to the moment of transition through the level of the input signal. Then for the next sub-band, set the initial level of voltage U_{B_i} equal to the penultimate value of the compensating voltage.

After conversion in the first sub-band, the number of apportioning is equal to:

$$n_1 = \frac{1}{\log\zeta_1}\log\frac{U_{IN}}{U_0} \tag{5}$$

and the penultimate level of compensating voltage (it is the initial level for the second sub-band):

$$U_1 = \zeta_1^{n_1-1}U_0. \tag{6}$$

On the completion of conversion in the second sub-band (second triggering of the comparator), the number of apportioning will be:

$$n_2 = \frac{1}{\log\zeta_2}\log\frac{U_{IN}}{U_1} \tag{7}$$

and the initial value of the compensating voltage in the third sub-band:

$$n_2 = \frac{1}{\log\zeta_2}\log\frac{U_{IN}}{U_1}. \tag{8}$$

On completion of conversion in the third sub-band (the third triggering of the comparator), the number of apportioning will be:

$$n_3 = \frac{1}{\log\zeta_3}\log\frac{U_{IN}}{U_2}, \tag{9}$$

and the initial value of the compensating voltage in the fourth sub-band:

$$U_3 = \zeta_3^{n_3-1}U_2 = \zeta_3^{n_3-1}\left(\zeta_2^{n_2-1}\left(\zeta_1^{n_1-1}U_0\right)\right). \tag{10}$$

Then the general formula describing a change in the compensation voltage will take the form:

$$U_k = U_{B_i} = U_0\prod_{i=1}^{m}\zeta^{n_i-1}. \tag{11}$$

The result of conversion N_1 with a one-sided descending sweep in the first sub-band is obtained by multiplying the number of apportionings reduced by one (n_1–1) by weight ν_1 of the first sub-band and recording this product in the result counter:

$$N_1 = (n_1 - 1)\nu_1$$

or

$$N_1 = \left(\frac{1}{\log\zeta_1}\log\frac{U_{IN}}{U_0} - 1\right)\nu_1. \tag{12}$$

After conversion in the second sub-band, multiply the number of apportionings reduced by one (n_2-1) by weight ν_2 of the second sub-band:

$$N_2 = (n_2 - 1)\nu_2$$

or

$$N_2 = \left(\frac{1}{\log\zeta_2}\log\frac{U_{IN}}{U_1} - 1\right)\nu_2. \tag{13}$$

Add the product to the content of the result counter, and after completion of conversion in the second sub-band, the following will be written in the result counter:

$$N = N_1 + N_2; \tag{14}$$

$$N = (n_1 - 1)\nu_1 + (n_2 - 1)\nu_2$$

or

$$N=\left(\frac{1}{\log\zeta_1}\log\frac{U_{IN}}{U_0}-1\right)\nu_1+\left(\frac{1}{\log\zeta_2}\log\frac{U_{IN}}{U_1}-1\right)\nu_2. \quad (15)$$

Finally, the result of conversion is equal to a sum of the mentioned products in individual sub-bands:

$$N=\left(\frac{1}{\log\zeta_1}\log\frac{U_{IN}}{U_0}-1\right)\nu_1+$$
$$+\left(\frac{1}{\log\zeta_2}\log\frac{U_{IN}}{U_1}-1\right)\nu_2+...+\left(\frac{1}{\log\zeta_m}\log\frac{U_{IN}}{U_{m-1}}-1\right)\nu_m. \quad (16)$$

In other words, the result of conversion is found as a sum of products of the number of apportionings by weights in each sub-band:

$$N=\sum_{i=1}^{m}(n_i-1)\nu_i$$

or

$$N=\sum_{i=1}^{m}\left(\frac{1}{\log\zeta_i}\log\frac{U_{IN}}{U_{Bi}}-1\right)\nu_i. \quad (17)$$

Consequently, with a descending sweep, the number of apportionings in each sub-band has a strict logarithmic dependence. The source code is formed taking into account the number and weight of each sub-band.

When converting with a ascending sweep, set the initial level of the compensating voltage in the first sub-band equal to the reference level, i. e. $U_{B_1}=U_0$. The reference value with a ascending sweep will correspond to the minimum possible input voltage.

Further conversion will be similar to the previous one and only sweep of the compensation voltage will be ascending.

4. 3. The process of conversion with replacement of the logarithm base with a ratio of capacitances and a two-sided sweep

The feature of the logarithmic ADC with a change of the logarithm base and a two-sided sweep consists in the following.

In each sub-band, change the compensating voltage U_k from the starting level U_{B_i} to the moment of transition through the level of the input signal. At the same time, set the starting level U_{B_i} in the i-th sub-band equal to the last value of the compensating voltage in the previous sub-band:

$$U_k=U_{B_i}=U_0\prod_{i=1}^{m}\zeta^{n_i}. \quad (18)$$

Note that the initial level in the first sub-band is equal to the reference level, i.e. $U_{B_1}=U_0$.

Let us consider in more detail the process of conversion.

On completion of conversion in the first sub-band, the number of apportionings will be as in expression (5) and the last level of the compensating voltage (which is the initial level for the second sub-band):

$$U_1=\zeta_1^{n_1}U_0. \quad (19)$$

With the help of multiplier, multiply the number of apportionings n_1 by the weight ν_1 of the first sub-band and record the product in the result counter:

$$N_1=n_1\nu_1 \text{ or } N_1=\frac{\nu_1}{\log\zeta_1}\log\frac{U_{IN}}{U_0}. \quad (20)$$

In the second sub-band, change direction of sweep of the compensating voltage from descending to ascending. After conversion in the second sub-band (the second comparator triggering), the number of apportionings will correspond to expression (7) and the last value of the compensating voltage in the second sub-band which will be initial value for the third sub-band:

$$U_2=\zeta_2^{n_2}U_1. \quad (21)$$

Using a multiplier, multiply the number of apportionings n_2 by the weight ν_2 of the second sub-band:

$$N_2=n_2\nu_2$$

or

$$N_2=\frac{\nu_2}{\log\zeta_2}\log\frac{U_{IN}}{U_1}. \quad (22)$$

In the result counter, subtract this product N_2 from the first product N_1. Therefore, after conversion in the second sub-band, the following will be recorded in the result counter:

$$N=N_1-N_2. \quad (23)$$

This value N differs from the value of result for a one-sided sweep in expression (14) in the sign between the codes N_1 and N_2 obtained in the first and the second sub-bands.

$$N=n_1\nu_1-n_2\nu_2$$

or

$$N=\frac{\nu_1}{\log\zeta_1}\log\frac{U_{IN}}{U_0}-\frac{\nu_2}{\log\zeta_2}\log\frac{U_{IN}}{U_1}. \quad (24)$$

In the third and other odd sub-bands, proceed with conversion in the same way as in the first sub-band (the descending sweep).

In the fourth and remaining even sub-bands, proceed with conversion as in the second sub-band (the ascending sweep).

Finally, logarithm N of the input signal U_{IN} will be written in the result counter after conversion is complete:

$$N=n_1\nu_1-n_2\nu_2+n_3\nu_3-n_4\nu_4...$$

or

$$N=\frac{\nu_1}{\log\zeta_1}\log\frac{U_{IN}}{U_0}-\frac{\nu_2}{\log\zeta_2}\log\frac{U_{IN}}{U_1}+$$
$$+\frac{\nu_3}{\log\zeta_3}\log\frac{U_{IN}}{U_2}+...+\frac{(-1)^{m-1}\nu_m}{\log\zeta_m}\log\frac{U_{IN}}{U_{m-1}}. \quad (25)$$

Consequently, conversion for a two-sided sweep occurs in odd sub-bands from the top down and in the even sub-bands from the bottom up. Accordingly, the source code of conversion is formed in turn with different signs.

5. Development of algorithms of analog-to-digital conversion with a replacement of the logarithm base with the ratio of capacitances

5. 1. Features of the conversion process

The height of step of voltage change in the accumulating capacitor determines the conversion error. The number of voltage U_{CN} steps in the accumulating capacitor depends on the ratio of input and reference voltages as well as on the logarithm base which, in turn, depends on the values of capacitances of the accumulating and apportioning capacitors. The height of each step is found from the logarithm base and the initial voltage value. Since the main idea of this work is to speed-up the converters based on the condenser cells, the value of the input voltage is reached first in large steps of U_{CN}. Reduce the step height in the subsequent sub-bands to obtain the sought error. Consequently, in order to evaluate metrological characteristics of converters, it is necessary to study how the step height changes from the change in the ratio of capacitances of the accumulating and apportioning capacitors.

Voltage on the accumulating capacitor can vary in different ways. For example, step-by-step change from big to small is a descending sweep. The descending sweep corresponds to the process of charge redistribution. If voltage in each cycle grows, it is a ascending sweep. It corresponds to the charge accumulation process in the condenser cell. Note that in accumulation of charge to obtain an ideal logarithmic conversion characteristic, active condenser cells should be used. For charge redistribution, the cells can be passive.

In each sub-band, there will be n_k of key switchings between the accumulating and apportioning condensers of the cell. The number of switchings of this key corresponds to the number of steps in the sub-band. Accordingly, conversion time of the whole device can be found as a sum of the products of multiplying the number of switchings n_k by the period of repetition of clock pulses.

Take the entire band of the U_{CN} voltage from 0 to 10 V. For a descending sweep, take 10 V as the initial value and 0.001 V for the ascending sweep.

In determining the source code of conversion, the weight ν_k of each bit and the result of conversion will correspond to the sum of products of multiplying the number of apportionings n_k by the corresponding weight ν_k. will also be taken into account

The feature of sweep formation for the FADC with replacement of the logarithm base with a ratio of capacitances is the user's assignment of a predetermined, fixed and identical number of apportionings n_k that corresponds to the number of steps for each sub-band of conversion. The required value of the logarithm base can be calculated as a ratio of the input and initial voltages in each sub-band in a power of $1/n_k$:

$$\zeta = \left(\frac{U_{IN}}{U_{B_i}}\right)^{1/n_k}. \quad (26)$$

The principle of sweep formation is simple for program implementation and protected from possible program looping.

When compiling algorithms of replacing the logarithm base with a ratio of capacitances as the initial values, the number of switches should be chosen. Each program also contains two cycles: an external cycle by number of sub-bands m and the internal cycle with the check of the compensating voltage value relative to the input voltage. Advantage of such an algorithm is the fixed number of steps of the internal cycle equal to n_{k+1}.

5. 2. The algorithm of analog-to-digital conversion with a replacement of the logarithm base and a one-sided descending sweep

Set the number of sub-bands D_1, D_2, D_3,..., D_m, minimum and maximum values of the input voltage and initial value of the compensating voltage. For the descending sweep, it is equal to the maximum value of the entire measurement band. Before the start of the external cycle, determine the first value of the logarithm base as a ratio of values of the input and the initial compensating voltages in a power of n_{k+1}. At the beginning of the external cycle, find the value of the compensating voltage taking into account the initial value and the value of the logarithm base. In the internal cycle, compare the value of the compensating voltage with the input voltage. If the compensating voltage is larger than the input one, make 10 steps downward. After reaching the moment of equality with U_{IN}, reset the value. Take the lower limit of the last step as the minimum input voltage. Take the upper limit of the last step as the maximum of the input voltage. Take a new maximum value for the initial value for the next sub-band. Calculate a new value of the logarithm base to reduce the step height.

Repeat the check if $U_k > U_{IN}$ and do the next 10 steps downward. Note that the upper limit of the last step is actually a penultimate, i. e. k-1 value of the compensating voltage. Accordingly, the minimum limit is the last the k-th value of U_k.

Fig. 1 shows voltage waveforms that explain operation of a converter with a variable logarithm base and a descending sweep.

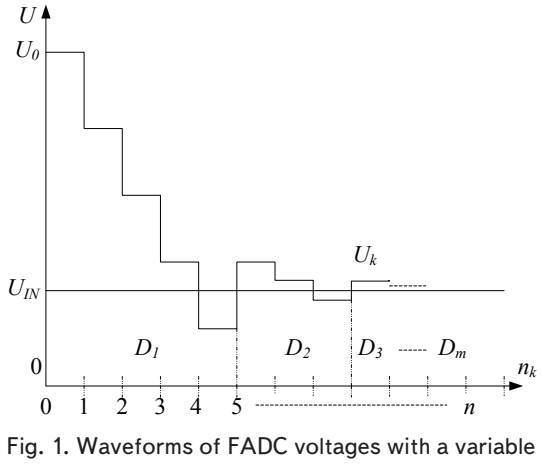

Fig. 1. Waveforms of FADC voltages with a variable logarithm base and a one-sided descending sweep

The developed algorithm for the variable logarithm base and a descending sweep is shown in Fig. 2.

Consequently, it is appropriate to use the algorithm with a descending sweep at high values of the input voltage. Since conversion takes place in downward steps, the fastest attainment of the desired value is possible.

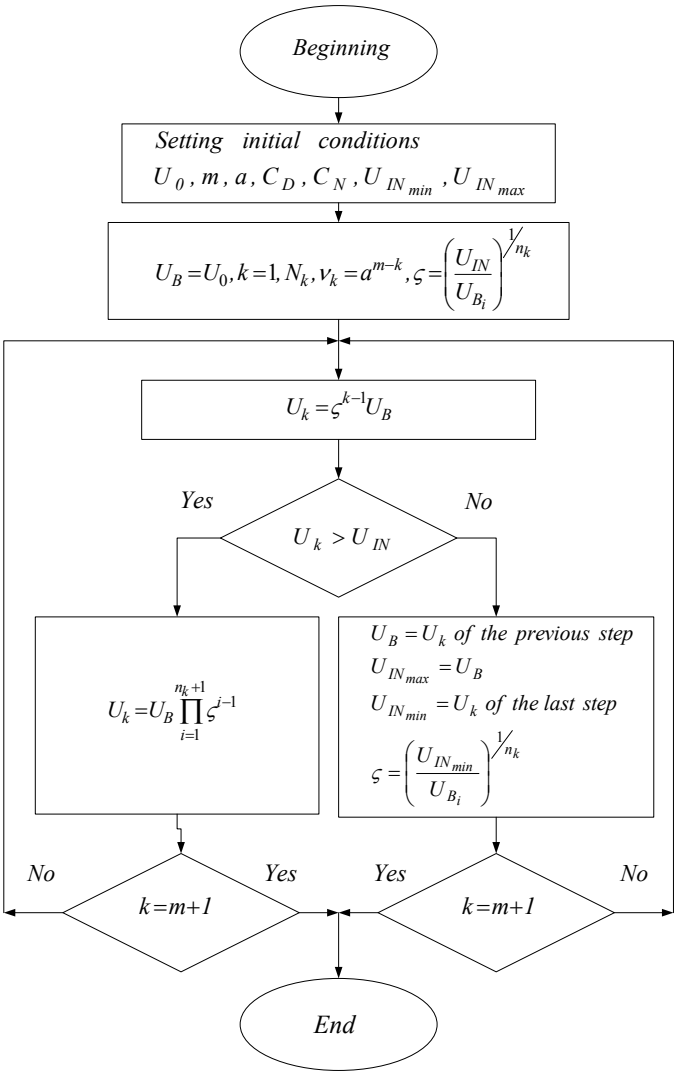

Fig. 2. The algorithm of conversion with replacement of the logarithm base with a ratio of capacitances and a one-sided descending sweep

5. 3. The algorithm of analog-to-digital conversion with replacement of the logarithm base and a one-sided ascending sweep

Formation of an ascending sweep corresponds to the charge accumulation process in the condenser cells. When working out an algorithm of such conversion, capacitance values of capacitors, the number of sub-bands, the minimum and maximum values of the input voltage are taken as starting conditions. This is the same as for the descending sweep but the initial value of the reference voltage will be other, close to the minimum value since the steps need to be made from the bottom up. Fig. 3 shows a voltage waveform that explains operation of a converter with a variable logarithm base and a ascending sweep.

The developed algorithm with an ascending sweep (Fig. 4) will differ from the previous condition in the internal cycle $U_k<U_{IN}$, and in that the initial value in the next sub-band will be equal to the bottom limit of the last step.

Consequently, it is expedient to use the algorithm with an ascending sweep if the predicted value of the input voltage is small because conversion takes place in steps upward.

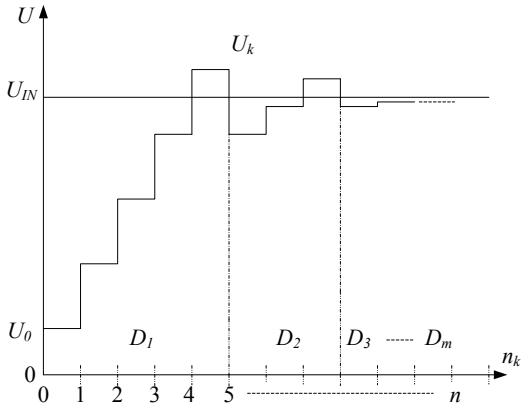

Fig. 3. The FADC voltage waveform with a variable logarithm base and a one-sided a ascending sweep

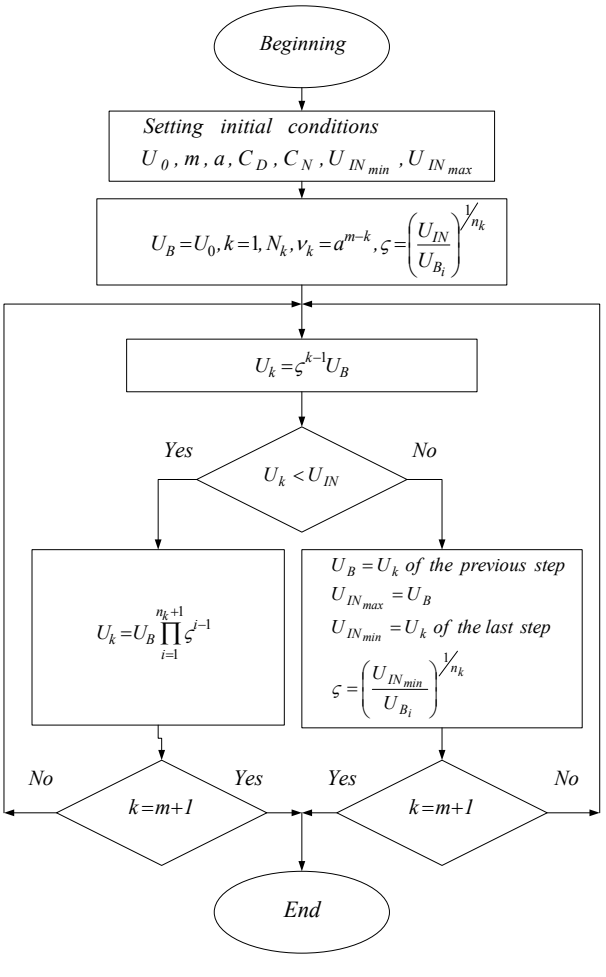

Fig. 4. The algorithm of conversion with replacement of the logarithm base with a ratio of capacitances and one-sided ascending sweep

5. 4. The analog-to-digital conversion algorithm with replacement of the logarithm base and a two-sided sweep

It is an interesting idea to combine a descending sweep with a descending one. In this way, conversion can be accelerated and reassignment of the maximum and minimum values in each sub-band simplified. The initial value of the compensating voltage in each sub-band will be the last value in the previous sub-band.

With each change of sub-band, the logarithm base will change to reduce the step height. The voltage waveforms explaining operation of a converter with a two-sided sweep are shown in Fig. 5.

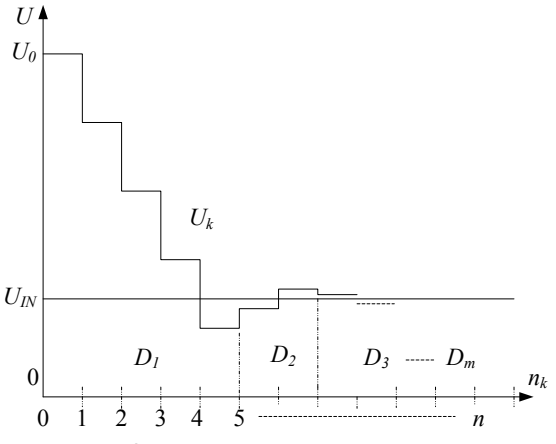

Fig. 5. The FADC voltage waveforms with replacement of the logarithm base and a two-sided sweep

Formation of the source code is of a special interest for conversion with replacement of the logarithm base and a two-sided sweep. It will include products of multiplying the number of apportionings by the weight of the corresponding band with a plus sign for a descending sweep and a minus sign for an ascending sweep.

As can be seen from the conversion functions (25) and the algorithm work, specifying a certain value of the logarithm base ξ in an *i*-th sub-band and increasing the sub-band weight v, the number of steps n_i can be reduced, that is, an increase in the speed of the developed converters. Instead, if the number of sub-bands increases, then the height of individual steps of the conversion characteristic and, accordingly, the error value can be reduced, that is, improvement of conversion accuracy is obtained.

The height of the conversion step sets the maximum value of absolute error. Its value is determined by the difference between two adjacent levels of the compensating voltage. For example, with ten steps in each sub-band, according to the expressions (19) and (21), the adjacent levels U_k:

$$U_{k_{i10}} = \varsigma_i^{10} U_{B_i}, \tag{27}$$

$$U_{k_{i9}} = \varsigma_i^{9} U_{B_i}, \tag{28}$$

$$\Delta U = U_{k_{i9}} - U_{k_{i10}} = \left(\varsigma_i^{9} - \varsigma_i^{10}\right) U_{B_i}. \tag{29}$$

The reference voltage value u_B decreases in each sub-band in accordance with (18). It sets the conversion boundaries.

In the first sub-band D_1, the whole band of conversion from 0 to 10 V is divided into ten steps. Therefore, the absolute error is one volt, and the overall error is about 10 %.

The second sub-band D_2 is reduced to the last step of conversion D_1, that is, units of volts. Therefore, the overall error will decrease to about 1 %. Similarly, decrease in the third sub-band will be approximately 0.1 % and approximately 0.01 % in the fourth sub-band.

The developed algorithm for conversion with a variable logarithm base and a two-sided sweep is shown in Fig. 6.

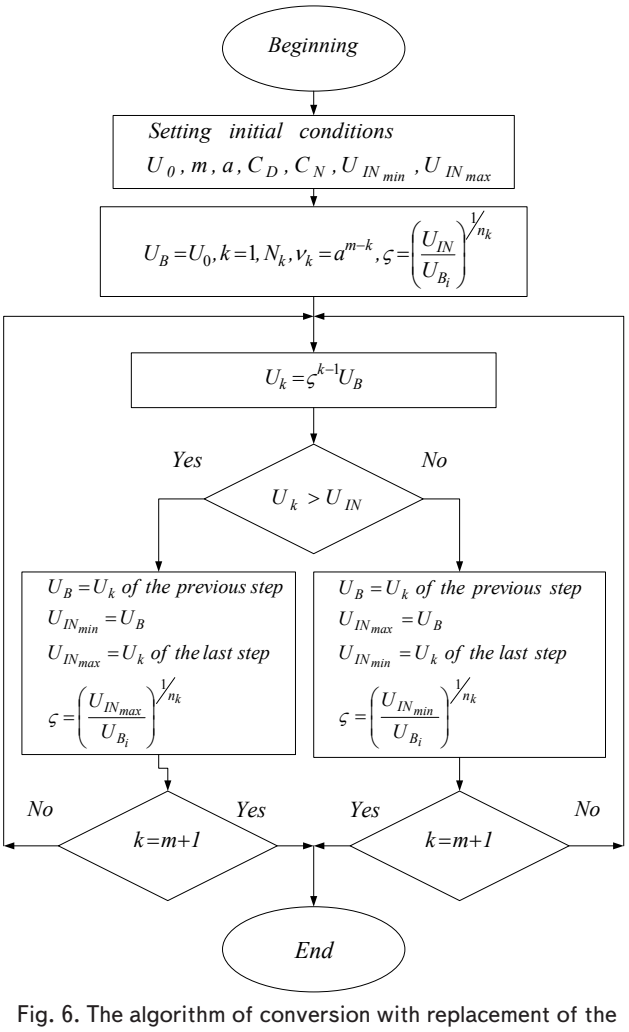

Fig. 6. The algorithm of conversion with replacement of the logarithm base with a ratio of capacitances and a two-sided sweep

Finally, when conversion is completed, logarithm *N* of the input signal U_{IN} according to expression (25) will be recorded in the result counter.

Thus, the algorithm of the two-sided sweep combines a descending and an ascending sweep. Reassignment of initial values in each sub-band is clearer and simpler in this algorithm. Its only drawback consists in the fact that the source code of conversion is formed alternately with opposite signs.

6. Discussion of study results

6. 1. Starting provisions

In the course of studying the functional analog-to-digital conversion with replacement of the logarithm base, ADC graphs were constructed with replacement of the logarithm base with a ratio of capacitances.

Modelling was carried out for various arbitrary values of the input voltage from 0 to 10 V, in a quantity not less than fifteen and evenly distributed throughout the band of the input voltage variation to make certain of correctness of the developed conversion algorithms.

The maximum number of apportionings in each of the sub-bands is n_k and the current value is denoted by i_k.

The change in voltage graphic presentation of modeling results is shown not by lines, but by discrete asterisks. This method most fully reproduces the discrete nature of change of the compensating voltage.

On the graphs, possible "empty" areas correspond to achievement of the value of the input voltage in less than 10 steps (apportionings). Moreover, accuracy for this sub-band is already maximal. Such an image is determined by the peculiarities of the display of graphs by the modeling envelope, and not by duration of the actual conversion in a condenser cell.

If the desired accuracy is achieved before conversion in a certain sub-band, then zeros are put in the code digits of the conversion result corresponding to it.

6. 2. The results obtained in modeling the analog-to-digital conversion with replacement of the logarithm base and a one-sided descending sweep

As already noted above, with a descending sweep, the initial value of the reference voltage U_0 and the compensating voltage resulting from it make the preset voltage 10 (or less when the value of the input voltage is reached earlier) steps down. At the same time, its level intersects with the input voltage level. In the next sub-band, instead of the initial reference value, take the penultimate value U_k and replace the logarithm base (respectively, the height of the voltage step) but again, make 10 (or less) apportionings.

Fig. 7 shows a graph for a one-sided descending sweep when the logarithm base is replaced with a ratio of capacitances and at U_{IN}=9.525 V.

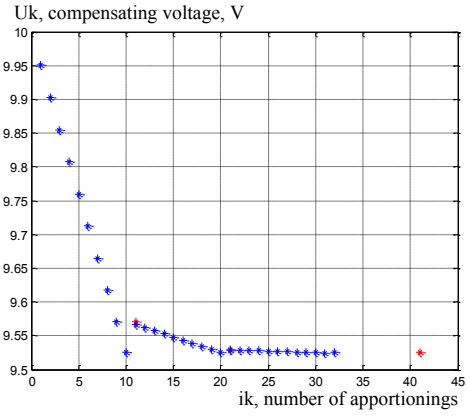

Fig. 7. Graph for a one-sided descending sweep with replacement of the logarithm base with a ratio of capacitances and at U_{IN}=9.525 V

As it can be seen, 10 apportionings were made in the first three conversion sub-bands and only one apportioning was suffice in the fourth sub-band.

Let us consider how the characteristic will change at a greater deviation of U_{IN} from the initial value of the reference voltage (Fig. 8).

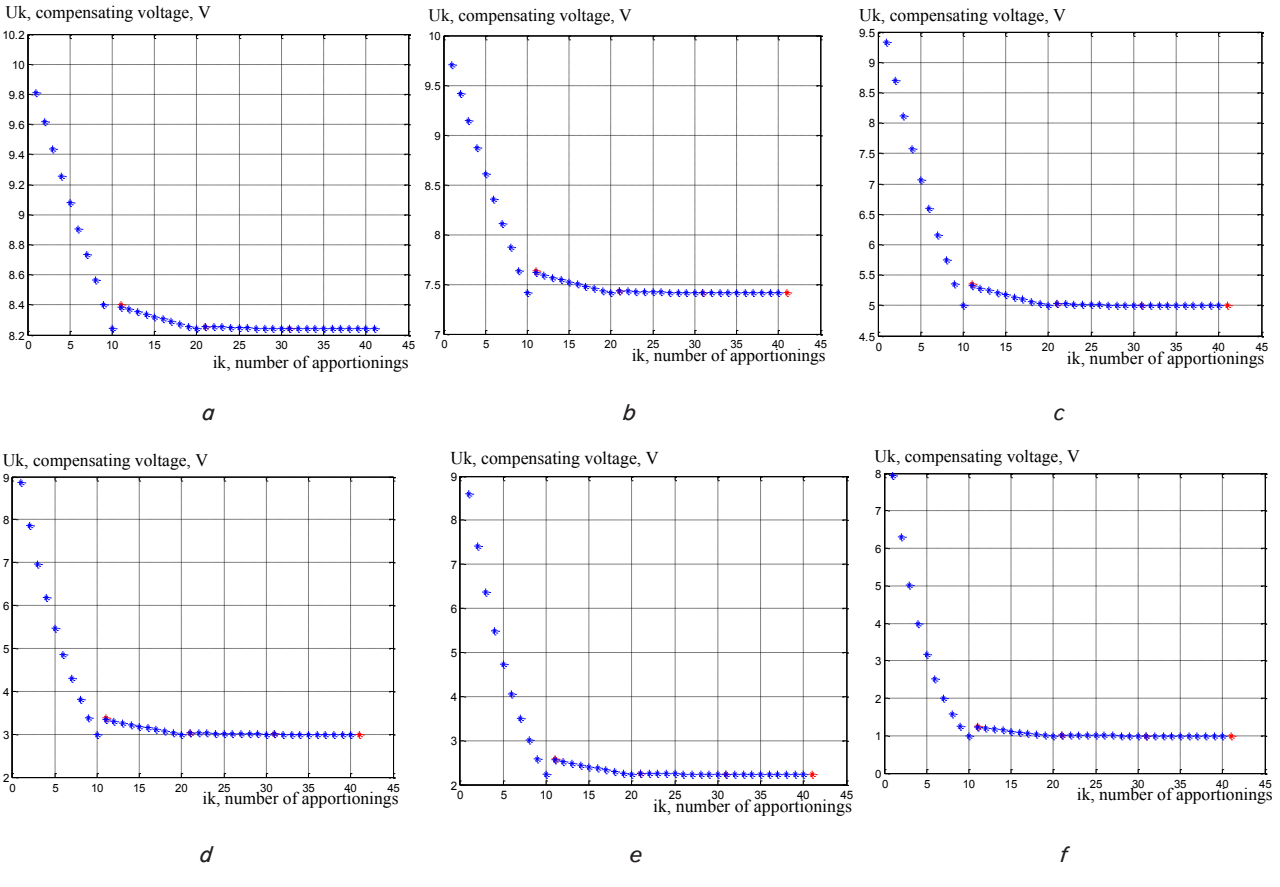

Fig. 8. The graph for a one-sided descending sweep with replacement of the logarithm base with a ratio of capacitances at values of the input voltage: U_{IN}=8.242 V (*a*); U_{IN}=7.413 V (*b*); U_{IN}=5 V (*c*); U_{IN}=3 V (*d*); U_{IN}=2.232 V (*e*); U_{IN}=1 V (*f*)

Consequently, with a one-sided descending sweep for various values of the input voltage, correct execution of the developed algorithm was obtained. Namely, in each sub-band, there are 10 apportionings and the errors are within the height of the last sub-band step. This is true even for the value U_{IN}=1 V farthest from the initial value of the reference voltage, 10 V (Fig. 8, *e*).

6. 3. Results obtained in modeling of analog-to-digital conversion with replacement of the logarithm base and a one-sided ascending sweep

Recall that with a ascending sweep, the minimum value should be taken as the initial reference voltage. It was 1 V in the subsequent studies. The steps of the compensating voltage are formed in upward direction. Fig. 9 shows a graph for a one-sided ascending sweep when the logarithm base is replaced with a ratio of capacitances and at U_{IN}=9.525 V.

Consequently, despite the maximum difference between the values of the input voltage U_{IN}=9.525 V and the initial compensating voltage U_0=1 V, the work clearly corresponds to the algorithm: conversion occupies all four sub-bands and the number of apportionings does not exceed 10 in each sub-band.

Let us consider whether this form of dependence will be preserved with other values of the input voltage.

It is logical to assume that with when the input voltage approaches the initial reference value, that is, with the decrease in U_{IN}, the number of apportionings in each sub-band will not increase but possibly decrease.

This is confirmed by the modeling results shown in Fig. 10. For example, with U_{IN}=6.135V, the first and second sub-bands contained 10 apportionings each, the third sub-band contained only 2 apportionings to approach the set accuracy and the fourth sub-band had one apportioning. In other words, at U_{IN}=3 V, the first sub-band contained 10 apportionings, the second sub-band contained only 3 apportionings to reach the set accuracy, and the third and fourth sub-bands already corresponded to the specified value of the input voltage. For one thirds of the studied values, it was unnecessary to apply all 10 apportionings in each of the four sub-bands and conversion of all values under study satisfied the preset accuracy after 40 steps.

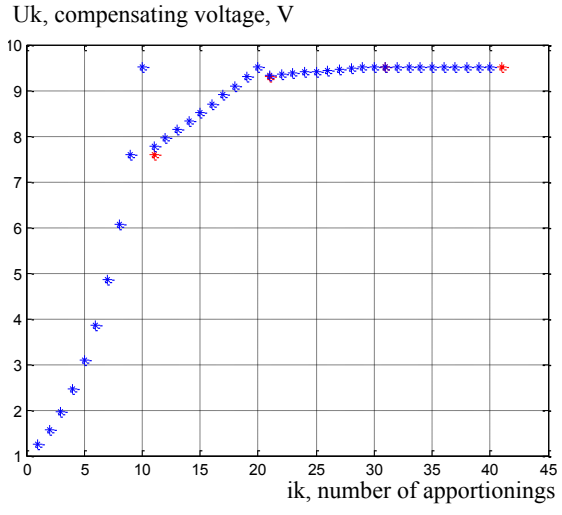

Fig. 9. Graph for a one-sided ascending sweep when the logarithm base is replaced with a ratio of capacitances and at U_{IN}=9.525 V

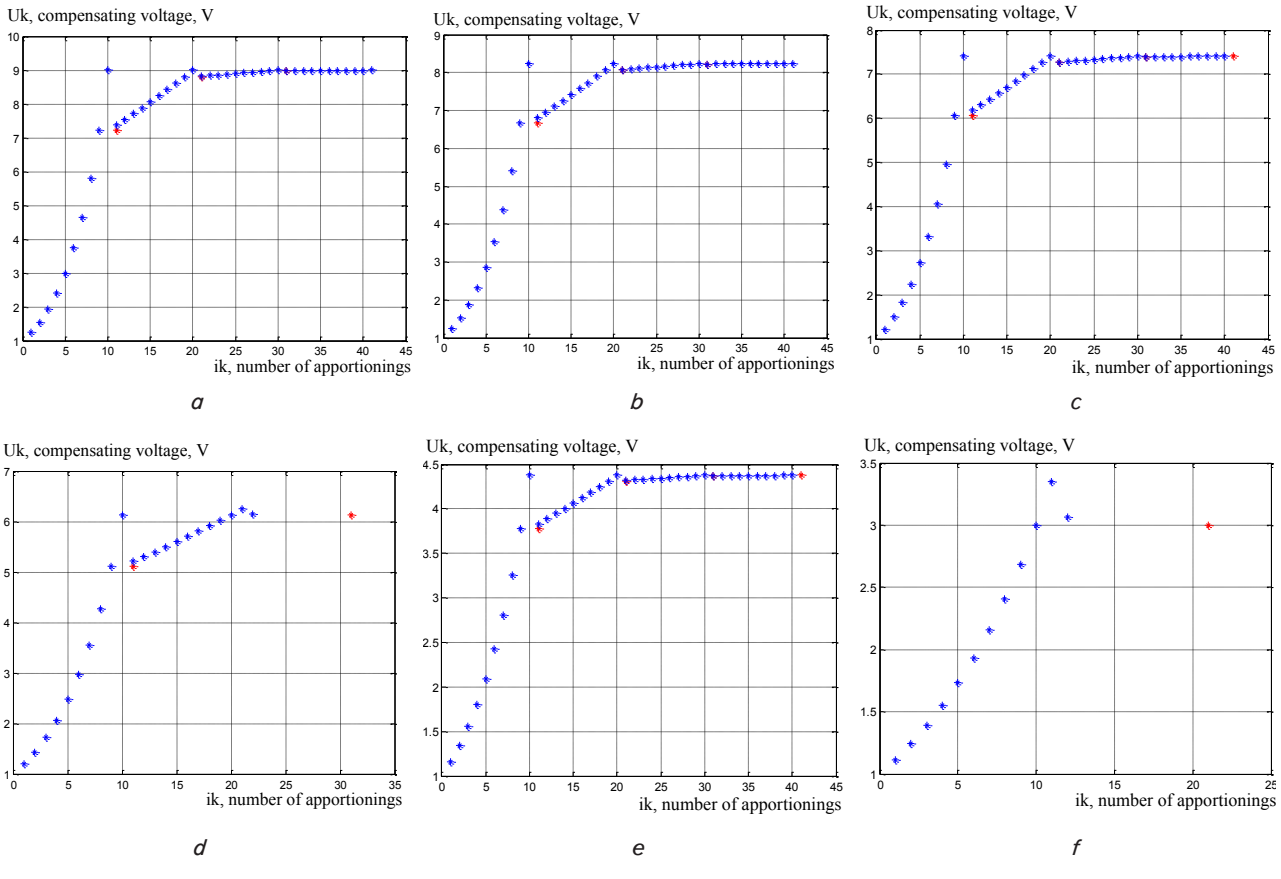

Fig. 10. Graph for a one-sided ascending sweep when the logarithm base is replaced with a ratio of capacitances at the values of the input voltage: U_{IN}=9 V (*a*); U_{IN}=8.242 V (*b*); U_{IN}=7.413 V (*c*); U_{IN}=6.135 V (*d*); U_{IN}=4.378 V (*e*); U_{IN}=3 V (*f*)

Consequently, the ascending sweep with replacement of the logarithm base with a ratio of capacitances ensures the correct work in accordance with the algorithm and stable apportioning numbers.

Even if the initial value of the reference voltage changed to 0.001 V at the input voltage of 1 V (Fig. 11), it can be seen that the number of apportionings in each sub-band increased but did not exceed 10 per sub-band.

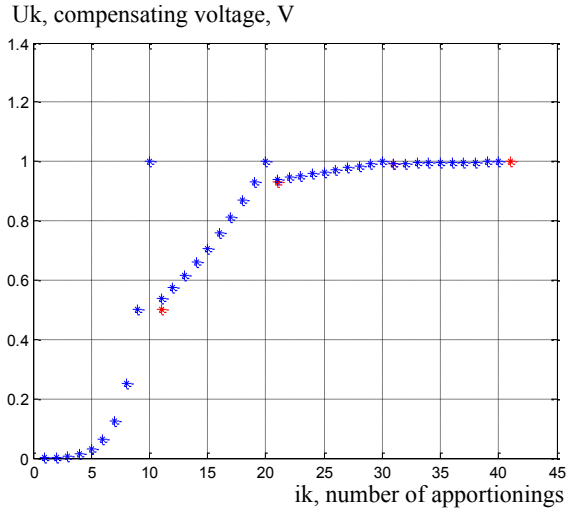

Fig. 11. Graph for an ascending sweep with replacement of the logarithm base with a ratio of capacitances and at U_{IN}=1 V and U_B=0.001 V

A conclusion can be drawn that the ascending sweep with a change of the ratio of capacitances is not inferior to the descending sweep both in accuracy or speed.

6. 4. Results obtained in analog-to-digital conversion simulation with replacement of the logarithm base and a two-sided sweep

Let us consider the results of combining a descending and a ascending sweeps in a two-sided sweep of conversion with replacement of the logarithm base with a ratio of capacitances.

Fig. 12 shows graphs for a two-sided sweep. All of them worked in four sub-bands. For individual values of the input value, in particular U_{IN}=9.525 V, U_{IN}=5.308 V and U_{IN}=1 V, there was a decrease in the number of apportionings in individual internal conversion sub-bands which did not impair stability of operation or accuracy of the obtained value.

Consequently, replacement of the logarithm base with a ratio of capacitances gives the required accuracy for a fixed number of steps. This has allowed us to recommend this ADC method for a faster performance without degradation of accuracy.

6. 5. Estimation of errors and speed of analog-to-digital conversion with replacement of the logarithm base with a ratio of capacitances

Based on the developed algorithms, conversion characteristics were elucidated and graphs and error values were obtained. Absolute errors were first obtained, and then, for ease of comparison, they were summed for each of the 15 input voltage values indicated above.

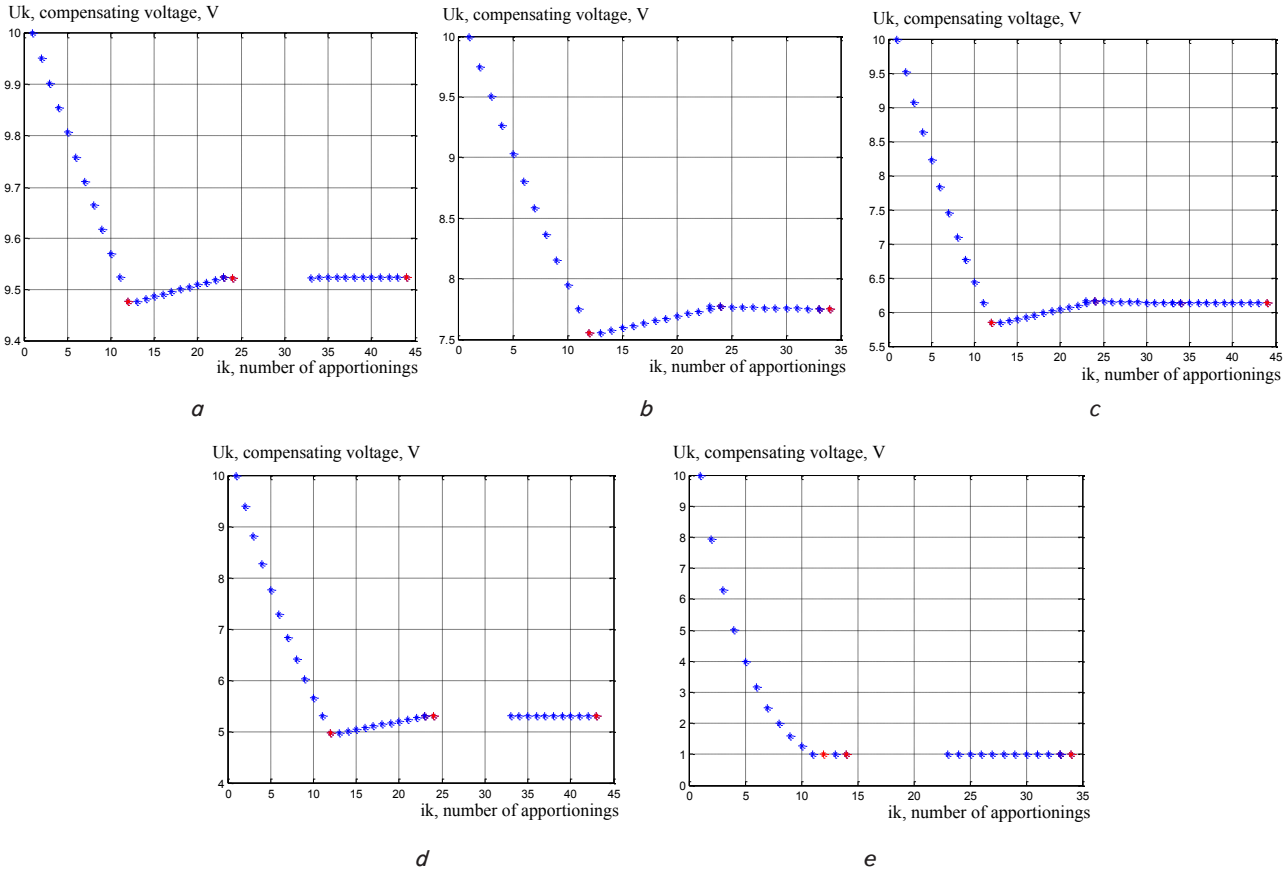

Fig. 12. Graph for a two-sided sweep with replacement of the logarithm base with a ratio of capacitances at the values of the input voltage: U_{IN}=9.525 V (*a*); U_{IN}=7.753 V (*b*); U_{IN}=6.135 V (*c*); U_{IN}=5.308 V (*d*); U_{IN}=1 V (*e*)

The absolute error of conversion was the difference between the input voltage U_{IN} and the compensating voltage U_k obtained during modeling. To obtain a summary error, the absolute error was divided by the nominal voltage value of 10 V and multiplied by 100 %.

It has been established that the error value varies in each sub-band. This corresponds to the idea of conversion. The value of the summary error for any input voltage in the band from 0 to 10 V does not exceed: 70 % in the first sub-band, 3.430 % in the second sub-band, 0.33268 % in the third sub-band and 0.0326 % in the fourth sub-band (Fig.13) For better presentation of the error values, the first least precise sub-bands D_1 and D_2 are not shown in Fig. 13.

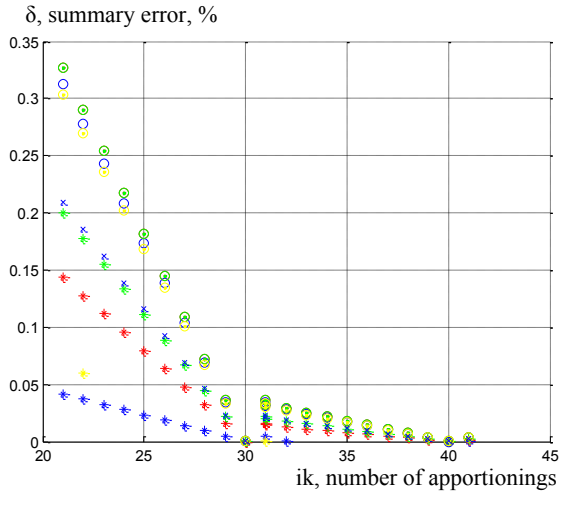

Fig. 13. Graph of the summary error in the third and the fourth conversion sub-bands

Note that the error decreases with each step in the sub-band. The maximum value will be at the first step of the sub-band and the minimum value will be at the last step. For example, the maximum error value in D_4 was at the 31st step and the minimum at the 40th step. The final conversion error should be taken exactly the value obtained in the last sub-band step. It is worth noting that the value of the summary error at the last point of conversion in the last, i.e. the fourth sub-band was further reduced by an order and amounted 0.005 % (Fig. 14). Color notation used in the error graphs: blue star for U_{IN}=9.5 V; red star for U_{IN}=8.242 V; green star for U_{IN}=7.413 V; yellow star for U_{IN}=6.13 V; blue circle for U_{IN}=5 V; red circle for U_{IN}=4.378 V; green circle for U_{IN}==3 V; yellow circle for U_{IN}=2.232 V; blue cross for U_{IN}=1.

The conducted study has shown that the errors with descending and ascending sweeps were practically the same. The error for the two-sided sweep was of the same order and differed in one or two less significant digits.

Conversion was also modelled for various numbers of sub-bands, in particular for three, four and five sub-bands. The obtained results confirmed that the increase in the number of sub-bands resulted in the error decrease. Calculated maximum errors did not exceed 0.3268 % when converting in three sub-bands. Conversion in four and five sub-bands has shown errors respectively less than 0.004635 % and 0.002 %.

The number of steps per each apportioning in each sub-band had a similar effect on the conversion accuracy. All calculations were made for n_k=10. However, modeling was also performed for various numbers of sub-bands with n_k=5 and n_k=15. It was found that 5 apportionings in each sub-band worsened accuracy: the summary errors made up 6.42 %, 1.42 % and 0.177 % respectively for three, four, and five sub-bands. Instead, an increase in the number of apportionings to n_k=15 has made it possible to obtain values of 0.3 %, 0.01601 % and 0.0001375 %, respectively.

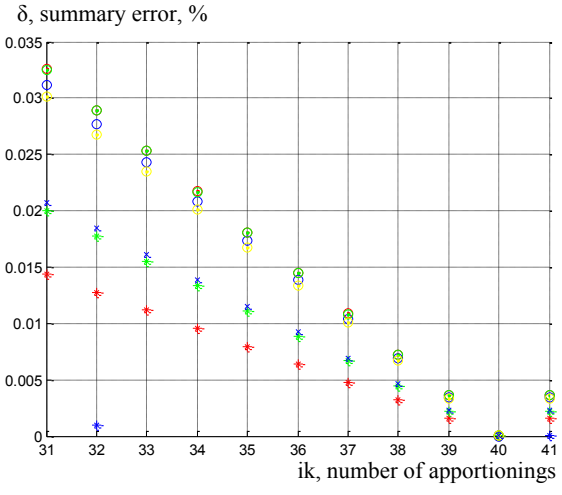

Fig. 14. Graph of the summary error in the fourth sub-band

However, an increase in apportionings in each band or an increase in the number of sub-bands of conversion leads to a decrease in speed. To compare, the conversion time did not exceed 40 T (T is the repetition period of clock pulses) for n_k=10 and four sub-bands, 60 T for n_k=15 and four sub-bands and 75 T for n_k=15 and five sub-bands. Thus, ten apportionings in each of four sub-bands were chosen as an optimal variant. Note that modeling for arbitrary seventeen values of the input voltage within 0–10 V has shown that all 40 steps of conversion were required for nine values and only 18 steps for six values. The last two values were converted in 33 and 39 apportionings.

7. Conclusions

1. Algorithms of replacement of the logarithm base with a ratio of capacitances in the analog-to-digital functional converter were worked out. The advantages of these algorithms are as follows:

– desired speed is determined by the user through setting the number of apportionings;

– accuracy can be specified by the number of sub-bands.

2. Modelling of work of a functional analog-to-digital converter has established the following:

– error did not exceed 0.005 % at 10 apportionings in each of four sub-bands;

– conversion time was less than 40 clock pulses or less than 100 μs.

3. Accuracy and speed of the developed algorithms practically did not differ from each other. Change of the logarithm base at a double-sided sweep is universal in use and recommended for any input values. Converters based on the developed algorithms exceed the known logarithmic ADCs in speed and are equal to the best of known analogues in accuracy.

4. The results obtained can be implemented in the process of designing automation, information, measurement, and computing means to increase speed at a high accuracy.

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