

*Представлений метод обробки зображень плям лазерних пучків для систем, які використовують сучасний та перспективний вид зв'язку з використанням атмосферно-оптичних ліній зв'язку (АОЛС). Метод дозволяє значно розширити використання лазерних технологій в системах передачі інформації за рахунок збільшення швидкодії, ефективності їх роботи і характеристик підсистеми позиціонування в них. Це важливо, оскільки під дією атмосфери (дощ, туман, тил, сніг) лазерний промінь деформується, а це, в свою чергу, впливає на якість результатів, отриманих від таких систем. Обґрунтовано необхідність фільтрації зображень, отриманих від передавача, шляхом використання адаптивних методів обробки інформації в паралельно-ієрархічних мережах. З метою пришвидшення обробки зображень плям лазерних пучків розроблена спеціалізована оперативна пам'ять (ОЗУ), що була використана в моделюванні розробленого методу обробки зображень плям лазерних пучків.*

*Виходячи з отриманих даних моделювання, результати прогнозування розташування приймача і ефективність роботи системи, отримані з представленим методом, на 15–20 % краще результатів, отриманих з використанням відомих методів. В результаті розробки представленого методу, вдалося скоротити кількість звернень до оперативної пам'яті в 2 рази, а отже зменшити навантаження на пам'ять. Удосконалена операція читання 2-портової пам'яті дозволяє формувати вектор зміщення паралельно-ієрархічного перетворення за один такт, розділивши ширину запису і зчитування шини даних, що, в свою чергу, збільшує ефективність роботи оперативної пам'яті*

*Ключові слова: паралельно-ієрархічні мережі, атмосферно-оптичні системи зв'язку, програмовані логічні схеми, лазерні пучки, класифікації зображень плям лазерних пучків*

## DEVELOPMENT OF A METHOD OF PROCESSING IMAGES OF LASER BEAM BANDS WITH THE USE OF PARALLEL-HIERARCHIC NETWORKS

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### 1. Introduction

To solve navigation, communications and other important tasks, laser beam profiling systems are currently used. In such systems, it is necessary to control the position of the energy center and the spot size of the laser beam. Examples of such systems are laser navigation systems and tracking of objects in military affairs, information transmission in atmospheric-optical communication lines, and others. In such systems it is very important to determine the direction of displacement of the laser beam as a result of exposure to the atmosphere. The solution of this problem is reduced, first of all, to determining the energy center of the spots of the laser beam, the coordinates of the center of gravity of their images and determining the contours with subsequent adjustment of the position of the receiving device [1, 2].

The use of laser technology in existing and promising information transmission systems can significantly

expand the number of transmission channels. For example, atmospheric-optical communication lines (AOCL) already exist and are actively using for the "last mile" [3]. However, even when such systems are installed on buildings, various oscillations can't be avoided, which lead to a displacement of the beam position between the receiver and the transmitter. This, in turn, necessitates the use of additional positioning tools.

In the process of tracking the transmitter by the receiving device (Fig. 1), the main tasks are processing the image of the laser beam spot in order to remove too noisy (deformed) images and finding the coordinates of the energy center of the image. The need to solve these problems is due to distortions under the influence of turbulence of air masses (rain, fog, dust, snow).

Known methods for processing images of spots of laser beams [4] are ineffective. Low efficiency is due to the complexity of the methods and their computational complexity.

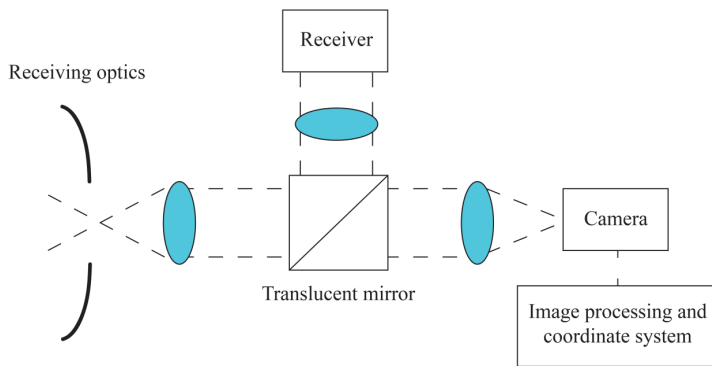


Fig. 1. Schematic illustration of a receiving device

In addition, stringent requirements are imposed on information transmission systems not only in terms of speed, but also in size and power consumption. Therefore, at present, AOCL uses hardware-based computing tools based on programmable logic integrated circuits (PLIC). A significant increase in the PLIC performance can be increased through the use of parallel-hierarchical networks [5].

Thus, the development of a high-speed method for processing images of spots of laser beams using parallel-hierarchical networks is relevant. The advantages of parallel hierarchical networks are their adaptability, the use of a simple mathematical apparatus, and the possibility of parallel computing.

## 2. Literature review and problem statement

In [1], the preferences for using laser technologies over radio waves are considered. It has been shown that laser technologies have a significant advantage, since the throughput can reach up to 2.5 Gbit/s, which is 10 times more than in radio waves, and the drawback is a strong dependence on atmospheric turbulence. In [2], the prospects of integrating AOCL with the existing Wide Area Network (MAN) and Local Area Network (LAN) are considered. AOCL provide less delay in the propagation of light, since the transmitters are on a direct line of sight compared to fiber-optic communication lines and the prospects of their integration. In [4], the authors investigate the “contour tape” method for classifying the image of laser beam spots, where the calculations are performed in stages in a single stream, which reduces the efficiency. In [6], atmospheric effects on the laser beam are studied in AOCL systems in various weather conditions. To improve the quality of the signal at different wavelengths, it is proposed to use a 4/4 system, that is, 4 receivers and 4 transmitters. In [7], the influence of temperature on the characteristics of laser beam transmission in the harsh climate of Qatar using the 2/2 system is studied. In [8], the effect of atmospheric dust of high concentration is studied using the 1/1 system, which can lead to loss of connection. The advantages of AOCL over existing communication lines are considered, including ease of installation, noise immunity, energy efficiency and the negative effect of the atmosphere on the laser beam. The influence of smoke and fog in the climate of Malaysia is studied in [9], rain, fog and scintillation state [10, 11].

Having studied the above literature, it is possible to conclude that the transmission of information using AOCL is very promising. But this raises the problem of the influence

of the atmosphere on the propagation of the laser beam and the adjustment of the position of the transmitter and receiver. To solve this problem, in [6, 7] it is proposed to increase the number of reception and transmission devices by 4 times and 2 times, but this will lead to a rise in price of such a system by 4 and 2 times, respectively. In [9–11], the attenuation of the power of a laser beam is studied under conditions of turbulence of the atmosphere of different terrain, which causes beam deformation of various types, as shown (Fig. 2).

Also, most of the known works do not mention the problem of loss of communication due to the need to adjust the position of the receiver. For example, during the operation of satellite-to-ground AOCL, a constant adjustment of the position of the receiving device relative to the position of the transmitter is necessary, for which the exit of the laser beam beyond the limits of the receiving lens will lead to a complete loss of communication [6–11].

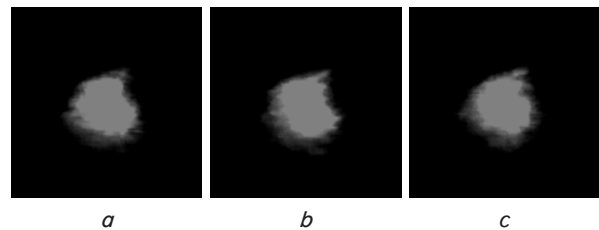


Fig. 2. A series of images of changes in the spot of the laser beam for the laser path:  
a – image 1; b – image 2; c – image 3

## 3. The aim and objectives of research

The aim of research is development and studying a method for processing images of spots of laser beams to filter noisy images and calculate the coordinates of the center of the spot of a laser beam using parallel-hierarchical networks.

To achieve the aim, the following objectives are set:

- use hierarchical networks in parallel to construct a method for classifying images of spots of laser beams and determining the coordinates of the center of the laser beam in AOCL systems;
- increase the RAM efficiency by reducing the number of requests;
- increase the RAM speed by creating a special logic memory circuit based on the created specialized register memory cell of the storage device;
- perform modeling of the developed algorithm based on PLIC, analyze the results.

## 4. Direct parallel-hierarchical transformation

To process images of spots of laser beams, it is proposed to use parallel-hierarchical (PH) neural networks. Networks in which information is encoded in the form of a hierarchy of a pyramidal structure, and transformations on individual elements are performed in parallel.

The principle of constructing a pyramidal hierarchical data structure can be defined as a sequence of data arrays of the same information field at different resolution levels:

$P=(A_0, A_1, A_2, \dots, A_L)$ , where  $A_k$  – the information field,  $k$  – the number of the resolution level (channel)  $k=\overline{0, l}$ .

In the case when the number of hierarchical levels is “0”, the conversion is carried out only at the zero level of conversion without the formation of tail network elements (output elements of the PH network).

The PH conversion algorithm is as follows.

Let’s consider the conversion  $G(M)=\{a_j | j=1, 2, \dots, m_1\}$ , applied in each processing channel. The original image  $M$  is represented by  $n$  segments (the number of image partitions  $M$ ) over which the  $G$  conversion is performed in each processing channel  $i, i=1, \dots, n$  simultaneously. Then the considered  $i$ -th image segment is  $M_i^1=\{a_{ij}^1 | j=1, 2, \dots, m_i^1\}$ , where  $m_i^1$  – the number of components in the  $i$ -th channel of the first level, and all considered segments can be represented in the form of matrix  $A_1$ :

$$A_1 = \begin{bmatrix} M_1^1 \\ M_2^1 \\ \dots \\ M_i^1 \\ \dots \\ M_n^1 \end{bmatrix} = \begin{bmatrix} a_{11}^1 & a_{12}^1 & \dots & a_{1m_1^1}^1 & x & x & \dots & x \\ a_{21}^1 & a_{22}^1 & \dots & \dots & a_{2m_2^1}^1 & x & \dots & x \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ a_{i1}^1 & a_{i2}^1 & \dots & \dots & \dots & \dots & \dots & a_{im_i^1}^1 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & x \\ a_{n1}^1 & a_{n2}^1 & \dots & a_{nm_n^1}^1 & x & x & \dots & x \end{bmatrix}, \quad (1)$$

where  $x$  denotes the absence of a component. The column index indicates the step of extracting the component, and the row index indicates the channel from which this component is taken. In the operator form, the analysis of the data specified by the matrix  $A_1$  is reflected on the second level using the transpose operation –  $T$ . That is, the initial matrix on the second level will be represented as  $A_1^T=T(A_1)$ . After the transpose is completed, the row index indicates the step number for extracting the component.

At the second level of processing, the transformation  $G$  is organized in such a way that it is possible to study correlations between components that are simultaneously extracted from the first level. This procedure applies to matrix rows  $A_1^T$ .

$$A_2 = G(A_1^T) = G(T(G(M))) = \begin{bmatrix} a_{11}^2 & a_{12}^2 & \dots & \dots & a_{1m_1^2}^2 & x & \dots & x \\ a_{21}^2 & a_{22}^2 & \dots & a_{2m_2^2}^2 & x & x & \dots & x \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & x \\ a_{i1}^2 & a_{i2}^2 & \dots & \dots & \dots & \dots & \dots & a_{im_i^2}^2 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & x \\ a_{n^2_1}^2 & a_{n^2_2}^2 & \dots & a_{n^2_{m_n^2}}^2 & x & x & \dots & x \end{bmatrix}. \quad (2)$$

The matrix  $A_2$  is formed at the second processing level after performing a temporary decomposition, in which each component  $a_{ij}^2$  is extracted at the stage  $t=i+j-1$ . If the matrix  $A_2$  is formed in such a way that the column index indicates the component extraction step, the same processing procedure can be applied at each next level of the hierarchy. This procedure is implemented as horizontal alignment of the rows of the matrix  $A_2$  and places the first non-empty element in each row on the main diagonal. The resulting matrix is designated as  $A_2^*$  and  $A_2^*=P(A_2)$ , where  $P$  – the line shift operator.

$$A_2^* = \begin{bmatrix} a_{11}^2 & a_{12}^2 & \dots & \dots & \dots & a_{1m_1^2}^2 & x & \dots & \dots & \dots & \dots & x \\ x & a_{21}^2 & a_{22}^2 & \dots & a_{2m_2^2}^2 & x & x & \dots & \dots & \dots & \dots & x \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & x \\ x & x & x & a_{i1}^2 & a_{i2}^2 & \dots & \dots & \dots & \dots & \dots & \dots & a_{im_i^2}^2 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & x \\ x & x & x & x & x & a_{n^2_1}^2 & a_{n^2_2}^2 & \dots & a_{n^2_{m_n^2}}^2 & x & \dots & x \end{bmatrix}. \quad (3)$$

The component  $a_{11}^2$  is the only one and therefore can be removed at the first stage of processing of the second level. This component in time is not connected with all other components of the second level and therefore is the output. It will also be an intermediate result of network processing, and – the only component elongated as a result of multi-stage processing at the second level. This component is formed from the matrix by removing its first column, and the components that remain are stored in the  $A_2^{**}$  matrix. This procedure is performed by applying the operator  $L$ , that is  $L(A_2^*)=a_{11}^2+A_2^{**}$ , a third-level matrix  $A_2^T$  is formed after the transpose operation  $T$  of the matrix, which can be written in the following form –  $A_2^T=T(L(P(A_2^*)))$ .

The described procedure is performed at each subsequent hierarchical level to the last level –  $k_{max}$ , in which the matrix  $A_{k_{max}}$  contains a single element. Then  $T(L(P(A_{k_{max}})))=\emptyset$ . Sequential use of the operators  $G, P, L, T$  can be represented as the execution of the operator  $F$ :

$$F(A_k^T) = T(L(P(G(A_k^T)))) = A_{k+1}^T. \quad (4)$$

The sequential application of the operator  $F$  can be represented as

$$F^k(A_1^T) = F^{k-1}[F(A_1^T)].$$

Then the whole multilevel process can be represented in the following operator form:

$$F^{k_{max}-1} \left[ T \left( G \left( \bigcup_{i=1}^n M_i \right) \right) \right] = \{a_{11}^k | k=2, 3, \dots, k_{max}\}. \quad (5)$$

Thus, the result of processing in a PH network is represented as an image vector containing a set of elements  $a_{11}^1 - a_{11}^k$ , which number is less than the initial number of elements in the investigated image [12].

The number of hierarchical levels is defined as follows:

$$N = R^1 + \sum_{t=1}^k P^{t+1} - (n^t - 1), \quad (6)$$

where  $R^1$  – the minimum number of diagonal sets at the 2nd level that generated the diagonal decomposition at this level.

$$P^t = \max \{R_1^t, R_2^t + 1; R_3^t + 2; \dots; R_{n^{t-1}}^t + n^{t-1} - 1\},$$

$R_{k-1}^k$  – the number of elements in the expansion of the set  $l^{k-1}$  at the  $k$ -th level.  $l^{k-1}$  – the number of the set (row) with the maximum dimension.  $n^{t-1}$  – the number of sets in the matrix  $A_{t-1}^*$ , that go to the  $t$ -level for further conversion.

If there are several sets with maximum dimension, then  $l^{k-1}$  – the highest sequence number of them. The number of hierarchical levels  $k$  is defined as follows:

$$k = \left\lfloor \frac{L}{2} \right\rfloor + 1,$$

where  $\lfloor \cdot \rfloor$  – the integer part of the number.

**5. Features of processing *P* and *T* operators.  
Reducing of RAM requests**

Creating hardware for processing parallel-hierarchical transformation is not an easy task and is described in the study [13] however, it does not solve the problem of working with memory, which is a bottleneck for many systems. Parallel hierarchical networks that require recurrent access to the data matrix are no exception.

However, the main operators for working with memory are *P*- and *T*-transforms, which are essentially read operations, which means they allow optimization, taking into account the structure of the RAM devices. An operation requiring a full processing cycle is a *G* operator (or *G* transformation).

The size of the necessary memory for the PH conversion can be significantly reduced by immediately allocating the maximum necessary memory of the matrix of certain sizes and overwriting it at each level of the PH conversion. At the same time, from the point of view of hardware implementation, it is necessary to evaluate such parameters as: the maximum number used in the calculation, the maximum dimension of the matrix obtained in the calculation process.

Table 1 gives an estimate of the maximum matrix size for the *G* transform algorithm. The simulation was carried out on a computer in Visual Studio 2010 [14] in the C# programming language. As test cases, artificially generated images using RNG are used [15]. Image color depth – gray: 8 bits.

Table 1

Characterization of the PH transformation using the minimum element in the operator *G*

Parameter	Matrix				
	4×4	16×16	64×64	128×128	256×256
Number of levels	15	144	578	1150	2140
Max Rows	6	56	253	512	964
Maximum number of columns	10	110	504	1022	1926
Maximum value	447	1680	4032	16000	64512
Execution time (ms)	41	189	4710	36000	251000

1. *T* – operator, or matrix transpose operation, requires rewriting each member of the matrix in accordance with formula (1) in a new matrix  $M^T$ .

Since the data storage is also performed in the form of a matrix in most RAM devices [16], it is quite clear that the transpose operation can be replaced by a simple permutation of the column and row address pointers. As a result, the rewrite operation is simply not needed.

In this case, the control device of such a memory also store data on the size of the matrix, in order to process only a given area of memory.

2. *P* – operator, or shift operator. According to formula (3), it requires rewriting each next line one position to the right of the previous one. This operator can be accelerated,

since only reading is required. And since the operators *L* and *T* follow it – formula (4), then by simply rearranging the address pointers it is possible to execute these operators in one pass.

An important consequence of such an operation is the reduction in required memory. The maximum number of diagonal sets does not exceed the number of columns, and therefore, when transposing such a matrix, the number of rows does not exceed  $2 \times N_d^k$ .

Then the maximum memory size is determined as:

$$M = (r_{\max})^2, \tag{7}$$

where *M* – the amount of memory,  $r_{\max}$  – the maximum number of rows during the PH decomposition of a matrix of a certain size (Table 1).

If to assume that the read operation of each cell is carried out in 1 cycle, then the total reading time of such a matrix is:

$$T = Endx \times Endy - 1, \tag{8}$$

where *Endx* and *Endy* – the boundaries of the matrix.

Thus, the combined reading operation reduces the number of accesses to RAM by approximately 2 times.

**6. Development of parallel structures of *P* and *T* transforms to increase RAM performance**

The main task in parallelizing the processes of access to memory is to increase the speed of the memory itself, as well as to increase the size of the access bus. Within the framework of this approach, two types of work with memory are possible:

- use of serial IC memory;
- creation of specialized RAM based on PLIC.

1. Modern PLIC chips are equipped with specialized interfaces for working with external memory chips (SRAM, SSRAM, QDR, DDR, etc.). Moreover, depending on the type of FPGA itself, there may be several such interfaces. Thus, it is possible to create external memory with a fairly significant bus width.

For example, the Stratix V chip [17] supports up to 4 DDR3 SDRAM x72 DIMMs, which results in a 288-bit data bus. Or, if set the cell size for the PH conversion to 16-bit (hereinafter referred to as the word), then let's get access immediately up to 18 words.

However, as can be seen from the Table 1, even for a 16×16 matrix, this is not enough to output 1 row. Thus, between the device performing operation *G*, an accumulation buffer must be introduced, which will form the input and output data.

At the same time, in modern storage devices, a memory area can be allocated for the entire matrix. And since the *G* conversion is an asynchronous process, it is enough to select 2 memory areas of the same size, one of which should be used for reading, and the other for writing.

At the next level, the PH networks are reversed. In addition, the presence of 2 (or more) physically separated memory ICs makes it possible to make reading and writing processes simultaneous.

Thus, the parallelization of access to external memory is determined by the ratio of the width of the data bus to the capacity of words used in the system.

2. When using external memory, the main problems are: the width of the data bus and the need to erase the cell after reading.

However, PLIC will allow to create logic circuits that are most consistent with the task. So, to solve the problem of the speed of access to the storage device, it is possible to create a specialized register cell of the storage device. The circuit of such a cell is shown in Fig. 3.

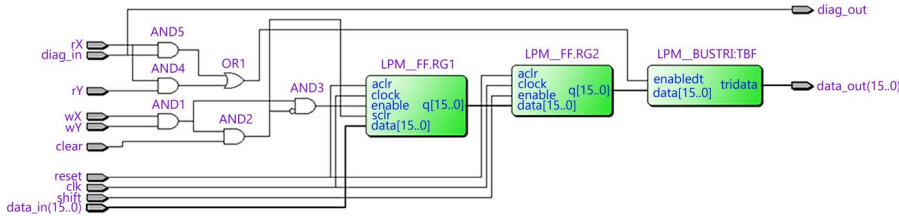


Fig. 3. Scheme of register memory cell

The cell consists of two registers RG1 – write register, RG2 – read register and output buffer with three states – TBF. The read bus and the write bus are separated, as well as their address inputs, and therefore the read and write operation can be done simultaneously (a description of the cell inputs is presented in Table 2).

The cell works as follows. After setting «1» to the reset input, the circuit is reset. By applying to the inputs wX, wY «1», it is possible to write data from the input bus. Further, having fed «1» during the 1st clock cycle, the data from the first register is transferred to the second input to the shift input.

Table 2

Description of the findings of the register memory cell

Output name	Direction	Description
Reset	input	Reset
Clear	input	Synchronous clear register entries.
Shift	input	The command to transfer data from register 1 to register 2
wX, wY	input	Address entries of a column and row, respectively, for a write operation
rX, rY	input	The column and row address inputs, respectively, for the read operation
Clk	input	Clock frequency
data_in	input	Input data bus
data_out	output	Output data bus
diag_in	input	Transpose read input
diag_out	output	Transpose read command output

Further, applying «1» to the inputs rX, rY, it is possible to read the data from the second register on the output bus. So far, at the inputs rX, rY «0», the output is in a high-resistance state due to a buffer with three states.

The input and, respectively, the output of diag\_in and diag\_out is used for the read operation with the combined operation P and T.

Modeling in the Altera Quartus 13.1 environment for a 16-bit bus shows that one such cell requires 35 logic elements. 32 of them are triggers. Maximum operating frequency is 250 MHz.

Further, it is proposed to construct memory matrices of any dimension from these cells (the limitation is the size

of PLIC and the specifics of its organization). Moreover, reading buses are combined horizontally – forming a reading vector. And the recording bus – vertically, forming a recording vector. Thus, the circuit forms a static vector RAM [18].

The advantages of such a memory device are:

- possibility of simultaneous and independent work of reading and writing;
- ability to carry out both scalar and vector operations;
- data transfer from the write register to the read register for 1 clock;
- possibility of both scalar and vector erasure of record registers;
- common data buses can also be combined in order to reduce the dimension of the input and output vector. It decreases speed, but operations with other blocks become possible smaller dimension;
- using the diag input, it is possible to read the matrix diagonals in vector.

### 7. Modeling of the developed method for the classification of images of spots of laser beams in PLIC

The above developments allow to create a structural diagram for classifying images and determining the coordinates of the center of the laser beam (Fig. 4), based on the use of a parallel-hierarchical network. The step-by-step algorithm for the method of calculating the coordinates and classification of spots of laser beams using the direct parallel-hierarchical transformation method is as follows:

- 1) receive data from the camera;
- 2) calculate the coordinates, and pre-filter the image;
- 3) save the filtered image;
- 4) find the tail elements of the PH transform;
- 5) find the correlation coefficient between the tail elements of the current image and the reference image;
- 6) if the correlation coefficient is greater than 0.95, then the coordinates of the center of the laser spot are updated with the data from p. 2, if not, then the previous ones remain.

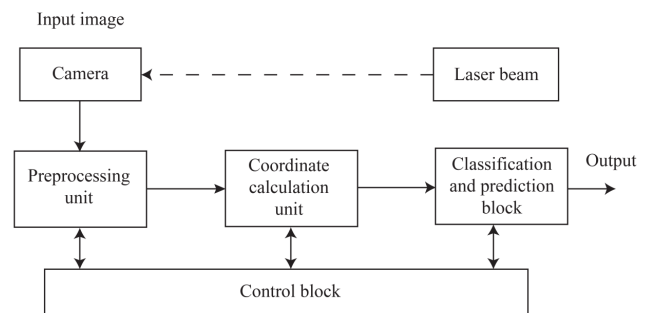


Fig. 4. The structural diagram of the processing of images of spots of laser beams

In order to verify the classification quality of the developed method, modeling was performed to process the obtained coordinates using some forecasting methods on real images (Fig. 5) of the visible 532 nm spectrum (green) provided by KIA Sistema (Russia).

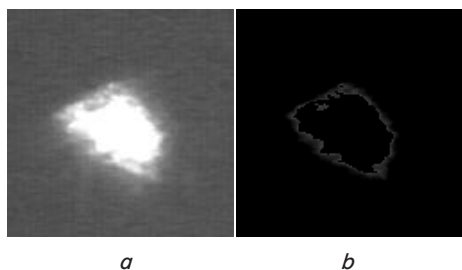


Fig. 5. Image of a spot of a laser beam: *a* – before processing; *b* – image contour after processing

As can be seen from Fig. 5, as a result of processing by the developed method, a clear contour of the image of the spot of the laser beam is obtained, which allows one to more accurately determine its energy center.

The simulation is carried out on the basis of the DE1-SoC board (Terasic Technologies L.L.C., USA) [19]. The simulation data are presented in Table 3.

Table 3

Simulation data

Parameter	Data
Total logic elements	9.632
Total registers	13822
Total memory bits	163619
DSP Blocks	21

The speed of the full circuit when processing real images of spots of laser beams amounted to (at a fundamental operating frequency of 100 MHz):

- using serial memory ICs – up to 25 ms/frame;
- using register memory – up to 7 ms/frame (an incomplete memory matrix is used due to resource limitation of the used PLIC).

The quality of the classification is checked by the ROC method [20] (Fig. 6). Metric values for the developed method: *TPR* = 71 %, *FPR* = 23 %.

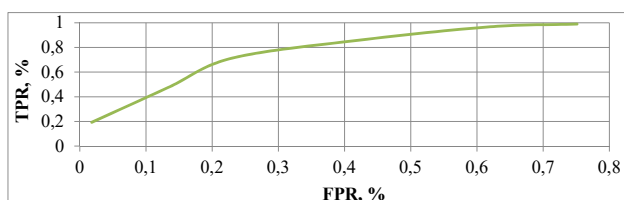


Fig. 6. ROC graph for the developed method

Let's compare the developed method with the contour tape method [4]. A comparative graph of errors for a segment of the route using the example of the X coordinate is presented in Fig. 7.

As can be seen from the Fig. 7, the developed method has a consistently lower average error than the contour tape method and allows more accurate calculation of the trajectory. The average error of the developed method is 0.47 %, the maximum error is 1.6 %, and the standard deviation is 0.36.

Table 4 presents data on the average forecast error of some forecasting methods during preliminary processing for the developed method and the contour tape method ( $\delta_{xav}$  – the average relative error of the method is calculated between the actual and forecasted value).

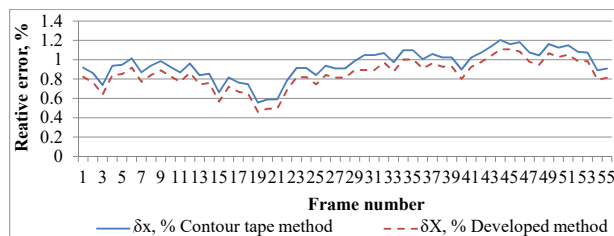


Fig. 7. Comparative chart of relative errors

Table 4

Comparative analysis of some forecasting methods for various types of data preprocessing

Forecasting method		
Method	Contour tape method, $\delta_{xav}$ , %	Developed method, $\delta_{xav}$ , %
Numerical methods [21]		
Exponential smoothing, additive model	0,87	0,85
Exponential damping smoothing	0,69	0,66
Autoregressive model	1,43	0,97
Neural networks [22]		
Radial basis function RBF S5	0,51	0,43
Line networkS5	0,46	0,37
Multilayer perceptron MP5-2-1 with another hidden layer	0,47	0,38

As the Table 3 shows, the results of calculations by the proposed method are 15–20 % better than the results obtained by the contour tape method.

### 8. Discussion of the results of the development of a method for processing images of spots of laser beams

The results are explained by the fact that in order to develop the method, parallel-hierarchical neural-like networks are used, the calculations in which are performed in parallel, which means faster, as can be seen from the simulation results presented in Fig. 5, 7 and Table 4. They are also explained by improved RAM performance.

A feature of the developed method, in comparison with the existing ones, is the speed of computation and processing of image data, as can be seen from the comparison in Table 4. As a result, it is possible to reduce the error and improve the results obtained by 15–20 %.

The main limitations of this study are the use of a less powerful DE1-SoC FPGA compared to SoCKit, which has its own 128Mb solid state drive and 1GB FPGA RAM instead of 64MB. Therefore, it can be argued that the results of the study could be improved.

The disadvantage of the developed method is that its implementation requires a more powerful hardware platform, since the calculations are performed simultaneously, which means that it is necessary to perform write and access to memory faster. Eliminating this problem, it is advisable to combine the shift and transpose operators, which reduces the number of queries by 2 times. To eliminate the problem of quick access to data, a specialized register

memory cell has been developed, on the basis of which it is possible to create a logical memory circuit most suitable for solving this problem.

Further development of the developed method can be improved on the hardware platform and applied in many specialized laser-optical systems, where it is necessary to improve the quality and speed of determining the coordinates of the image coordinates of the spots of laser beams. It also initiates hardware improvements for the most parallel hierarchical networks. In further studies using this method, one may encounter the complexity of the mathematical base and the insufficient capacity of the hardware platform.

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## 9. Conclusions

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1. Based on the basis of parallel-hierarchical neural networks, a method for processing and classifying laser beam

spots and determining the coordinates of the center of the laser beam in AOLS systems is developed, the calculations in which are performed in parallel. Therefore, the calculations will be performed faster, with sufficient hardware platform power, as can be seen from the simulation results presented in Fig. 5, 7 and Table 4.

2. The method of direct parallel-hierarchical transformation is further developed, upon implementation of which it is proposed to combine the shift and transpose operators for a parallel-hierarchical network, which reduces the number of memory accesses by 2 times.

3. The operation of reading 2-port memory is improved, which allows to create a displacement vector of parallel-hierarchical transformation in one clock cycle.

4. Having built the model on the basis of the developed method and having analyzed the work using the ROC method, it is realized that the proposed one is 15–20 % better than the contour tape method.

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