

The paper describes the types of multilevel pulse-width modulation, as well as methods for obtaining control signals for the inverter power switches for each of the types. The dependence of the harmonic composition of the output voltage of the inverter on the number of levels and the switching frequency of the keys of each level is analyzed. By modeling, the dependences of the transistor junction temperature on the number of voltage levels, switching frequency and load power are determined. The power switching system of an inverter with phase-shifted pulse-width modulation in high-frequency mode is analyzed, the dependence of switching losses on inductance is investigated. The ways of solving or improving the control systems of the conductivity losses of the converter flowing through the primary winding of a high-frequency transformer during the free-running period are formulated. The importance of this direction for the technological development of the economy, where efficiency improvements can lower individual utility bills, create jobs, and help stabilize electricity prices and volatility is shown. The most important stage of inverter design is called structural synthesis stage – the choice of topology and modulation algorithm that will ensure the greatest efficiency of the device. In addition, since the efficiency and reliability of inverters depend on the efficiency and reliability of secondary electricity consumers, the task of optimizing inverter circuits is a cornerstone for the effective development of technology and economy. The maximum dynamic power loss at a PWM frequency of 1 kHz reaches only 80 watts compared to the static power loss value of 800 watts

Keywords: multilevel inverter, pulse-width modulation, output voltage, energy efficiency, total harmonic distortion, switching frequency, transition temperature

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1. Introduction

Recently, multilevel pulse-width modulation (PWM) inverters have become increasingly common, combining both pulse-amplitude modulation (PAM) and PWM modulation. In such converters, the voltage at each level of the PAM is a PWM signal, which allows you to get an output signal close to the sine wave. When powering heavy-duty appliances from a multi-level inverter, the load is distributed across levels, which allows the use of less powerful and compact valves. Due to the rapid development of the semiconductor power and microelectronic base, which allows implementing complex control algorithms, multi-level inverters are becoming more and more popular. This is also confirmed by modern publications [1]. Multi-level voltage inverters represent a highly efficient solution in the high-voltage energy market. Currently, power semiconductor devices for alternating current electric drives are actively used, static reactive energy compensators for the transmission of direct and alternating current electricity.

The peculiarity and main advantage of multi-level inverters compared to classical two-level inverters is that by increasing the semiconductor elements in the circuit, the following results can be achieved:

1) the possibility of obtaining high output voltage using standard low-voltage semiconductor elements, such as insulated-gate bipolar transistor (IGBT) modules without resorting to the need for high-voltage expensive semiconductors;

ANALYSIS OF POWER LOSSES IN MULTILEVEL PULSE-WIDTH MODULATION INVERTERS

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2) high quality of the supply network, striving for an ideal sine wave due to the multi-stage output voltage.

Many other possibilities follow from these fundamental advantages. We will try to analyze these features in more detail.

The ability to generate high voltage allows you to effectively regulate power flows between power systems, stabilize voltage on power lines.

The main advantage of multi-level voltage inverters is the high quality of the output voltage, as evidenced by the low level of THD (total harmonic distortion) [2]. At the same time, the use of more expensive converters of this type is not justified in all cases. The PWM algorithm used in conventional inverters can also be used in multi-level inverters. Completely different MLI topologies for use as a converter for electric drives, a cascade inverter with discrete direct current sources and a subsequent diode-locked converter [3]. And also, as for single-level PWM, two-way modulation methods using several triangular carrier signals and one modulating sinusoidal or sinusoidal signal with third harmonic premodulation have become the most common. This is due to the lower content of parasitic harmonics in the output voltage spectrum of such an inverter. The efficiency of the inverter may vary depending on the input power and voltage of the photovoltaic array. Three factors affecting the efficiency of the inverter were analyzed. The first of them was the effect of the duration of the inverter [4]. The multi-stage output voltage of a traditional inverter is obtained with the correct

arrangement of power semiconductor switches. Power semiconductor switches in the design of traditional MLI (multi-level inverter) are controlled directly by a sequence of pulses obtained using PWM methods with multiple carriers. These MLIs do not require any intermediate circuit to convert the received pulse sequence into the desired pulse sequence. Due to the larger number of electrical and electronic components, various parameters such as power loss, total harmonic distortion (THD), efficiency, etc. affect traditional MLI designs. To overcome these disadvantages of traditional MLI, many researchers are introducing reduced switch multilevel inverters.

The use of the inverter topologies discussed above and their modifications can significantly improve the harmonic composition of the output voltage of the inverter and thereby ensure the requirements of consumers for its sinusoidality. However, a wide variety of topologies and modulation algorithms creates a problem of choice when designing an inverter, this problem remains relevant.

2. Literature review and problem statement

In [5], researchers have proposed various reduced switch multilevel inverter (RSMLI) systems with their switching sequence and PWM control methods. However, RSMLIs switching operations are not like regular MLIs, which are the main problem of switch management. Logical equations are proposed for the operation of RSMLIs using PWM methods with multiple carriers, such as alternative phase resistance distribution, phase resistance distribution and phase distribution. To control a separate switch in symmetric and asymmetric RSMLI, logical operators are used to obtain the required sequence of pulses from the sequence of the PWM method, and their analysis is absent in the works. The proposed methodology can be applied to photovoltaic systems for efficient operation. The proposed methodology and binary representation of the PWM method are analyzed on various RSM for a seven-level output voltage for the operation of each individual switch.

The paper [6] presents the theoretical principles of operation of two inverter topologies. As already discussed, push-pull and H-bridge topology of inverters has advantages and disadvantages. The design of the inverter in a photovoltaic system is based on the load applied to this system. These theoretical operations are important when designing an inverter to make solar technology more feasible. The push-pull topology was chosen for designing an inverter for low-load applications in a photovoltaic system. Push-pull topology was the first step in the technology of electronic inverters. The advantage of this topology is the simplicity of the overall scheme and cost-effectiveness in production. But the main problem is that the current in the transformer suddenly changes direction.

In the project [7], the research, design and modeling of an interconnected single-phase H-bridge inverter were carried out. The inverter was modeled and recommendations for the implementation of a hardware prototype were given. The purpose of this project was to draw conclusions about whether an inverter produces fewer lower harmonics than a rectangular inverter. The control signals for multi-stage inverter designs are more complex than the control signals of a rectangular inverter, but the cleaner output voltage of multi-

stage inverter designs makes them more suitable for modern inverter applications, such as converting direct current from solar panels to pure alternating current.

In [8], the crystal of the transistor was used to eliminate unwanted harmonics at the output of CHB-MLI. This helps to estimate the optimal switching angle by solving a nonlinear transcendental equation, which helps eliminate lower-order harmonics and therefore improve the output voltage THD. Therefore, the crystal for CHB-MLI can be effectively used in many applications, such as electric vehicles and solar photovoltaic systems.

Previously, in a symmetrical cascade inverter, each H-bridge cell in a multi-level cascade H-bridge inverter has the same DC input voltage with four power switching devices. To increase the output levels of AC voltage, it is necessary to increase the DC inputs and switching devices. Consequently, the total cost of the system will also increase [9]. The amplitude of the output voltage pulses is half of the DC input voltage [10]. The rapid improvement of power electronics switches increases the need for power converters with high performance and power quality [11]. A multi-level inverter can achieve a basic and high switching frequency based on PWM [12]. Increasing the output voltage levels of a multi-level inverter makes it possible to improve the power quality of the AC output voltage and reduce THD [13]. It is unable to generate zero output voltage intervals for nonresistive loads [14], gives THD results lower than in the ZL state. The system is formed in such a way as to provide different voltage levels and minimal THD compared to the conventional type. There is a system distortion for multiple levels and RL loads. The results of the system explained the effectiveness of the proposed system with N states ZL. The proposed MI with them as a PWM controller may well be used in industry, since low THD is required.

In [15], a new 5-level T-type inverter based on SC was proposed. Thanks to the integration of only two SCS, the proposed topology retains the advantages of existing 5-level NPC/T-type SC-MLIS, such as doubling the use of DC line voltage (compared to classic T-type or ANPC inverters) and natural capacitor voltage balancing. More importantly, it eliminated the two most noticeable drawbacks in all existing SC-MLIs, including the problem of current surges and large voltage ripples on the capacitor. Smooth charging technology has been implemented for all SCS, not only to eliminate current surges, but also to ensure continuous charging of the SCS during operation to minimize voltage ripples and capacitor size. The corresponding theoretical analysis, design calculations, modeling and experimental tests are presented to verify the viability and practicality of the proposed topology.

3. The aim and objectives of the study

The aim of the study is to compare different types of inverters and develop an inverter with the lowest switching losses.

To achieve the aim, the following objectives were solved:

- to compare the harmonic composition of the output voltage of a multilevel inverter;
- to determine the dependence of power losses on the junction temperature when using multilevel PWM inverters;
- to simulate a high-frequency inverter with smooth switching with a phase shift and a step-up converter.

4. Materials and methods

We will consider the circuits of a multilevel PWM inverter consisting of series-connected bridge circuits (cascade bridge circuit) and use a multilevel PWM with a phase shift of carriers. This topology has the following advantages: easily scaled, contains no elements other than IGBT modules, which facilitates the task of estimating installed capacity and cost, most often used in practice.

The object of the study is the processes in inverters operating in soft switching modes.

Due to the large nomenclature of IGBT modules, on the basis of which modern voltage inverters are built, it is possible to apply almost any inverter topology to power an arbitrary consumer – the task in this case will only be to choose the right module. However, it does not follow from this that the resulting inverter will be optimal in terms of cost, installed capacity and weight and size indicators.

This task involves determining the operation modes of inverters in which the use of a specific implementation of the inverter is optimal in terms of weight, size and cost indicators, which is an actual component of the inverter design process.

The solution of the task is important both from a practical and scientific point of view. From a practical point of view, it is important to achieve this by automating the design process, and automation is not possible without systematic knowledge about the effectiveness of using a particular inverter topology in various operating modes. From a scientific point of view, the availability of such information makes it possible to determine the operating modes of inverters in which most of the existing topologies are ineffective, and to propose specific ways to optimize such inverters.

Due to the large variety of schemes and modulation algorithms, solving the problem in general requires a lot of time. Therefore, it was decided to limit it to comparative analyses of the most common inverter circuits and prove the possibility of solving such a problem.

Three methods of multilevel PWM are most common in the literature [16]: multilevel PWM based on a carrier signal, selective harmonic suppression and multilevel space-vector modulation. Multilevel modulation algorithms are easier to consider based on the SCHBI (series-connected H-bridge inverter) topology, although they can be transferred to two other common topologies of multilevel inverters. With SCHBI (series-connected H-bridge inverter), each module can generate voltage with levels $-U_{DC}$, 0 and U_{DC} . Thus, a circuit consisting of M modules can form n_{level} of various voltage levels in the range from $-MU_{DC}$ to MU_{DC} , in U_{DC} increments (Fig. 1).

An inverter with M (number of separate DC voltage sources) modules is usually called a level inverter, since the number of output voltage levels is a more important indicator for the consumer compared to the number of modules. The number of level levels is related to the number of modules by the following ratio:

$$n_{level} = 2M + 1. \quad (1)$$

Several different modulation methods have been proposed in the literature. Conventional two-level high-frequency modulating inverters for electric drives have many

problems related to their switching frequencies, which create a common-mode voltage and a high voltage correction rate (dU/dt) on the motor winding. The development of multi-level inverter highlights these issues, so their devices will switch at the lowest possible frequency. In all level shifter pulse-width modulation (LSPWM) methods, the carrier signals have an f_{CAR} frequency equal to the frequency of the output voltage pulses, called the apparent switching frequency f_{sw} , and a voltage amplitude equal to the DC link voltage. The reference voltage, on the other hand, can have values ranging from $-MU_{DC}$ to MU_{DC} . To cover the entire voltage range, the carriers are shifted vertically, so that the carrier of the first module covers the range from zero to U_{DC} , and the second covers the range from U_{DC} to $2U_{DC}$, etc. The last module covers voltages from $(M-1)U_{DC}$ to MU_{DC} .

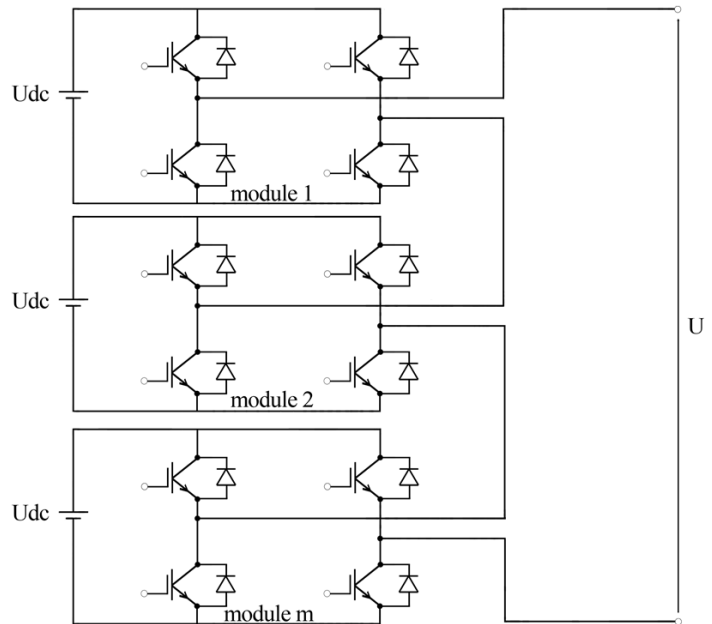


Fig. 1. Diagram of a cascade bridge inverter

Fig. 2 [16] illustrates the distribution of carriers with respect to the reference voltage, according to the described method. The figure also shows the generated voltages of each of the modules and the output voltage of the inverter.

Switching moments are determined by comparing the reference signal with the modulating one. The state of the module is defined as $+U_{DC}$ if the reference is higher than the positive carrier, and 0 otherwise. For negative values of the carrier signal, the opposite is true:

$$U_{MOD} = \begin{cases} U_{DC}, & u_{phase} > |u_{CAR}|, \\ -U_{DC}, & u_{phase} < -|u_{CAR}|. \end{cases} \quad (2)$$

A comparison of the load of SCHBI modules when using a multilevel PWM with a level offset shows that module M is used at short intervals during the period, while the first module is used almost all the time [17]. Consequently, the DC circuit capacitors of different modules are loaded differently, as a result of which the voltage balance between them is not observed. When the energy accumulated in the inductive part of the load is returned, most of it is sent to the capacitor of the first module, which can lead to its breakdown, since the voltage in the DC circuit increases sharply.

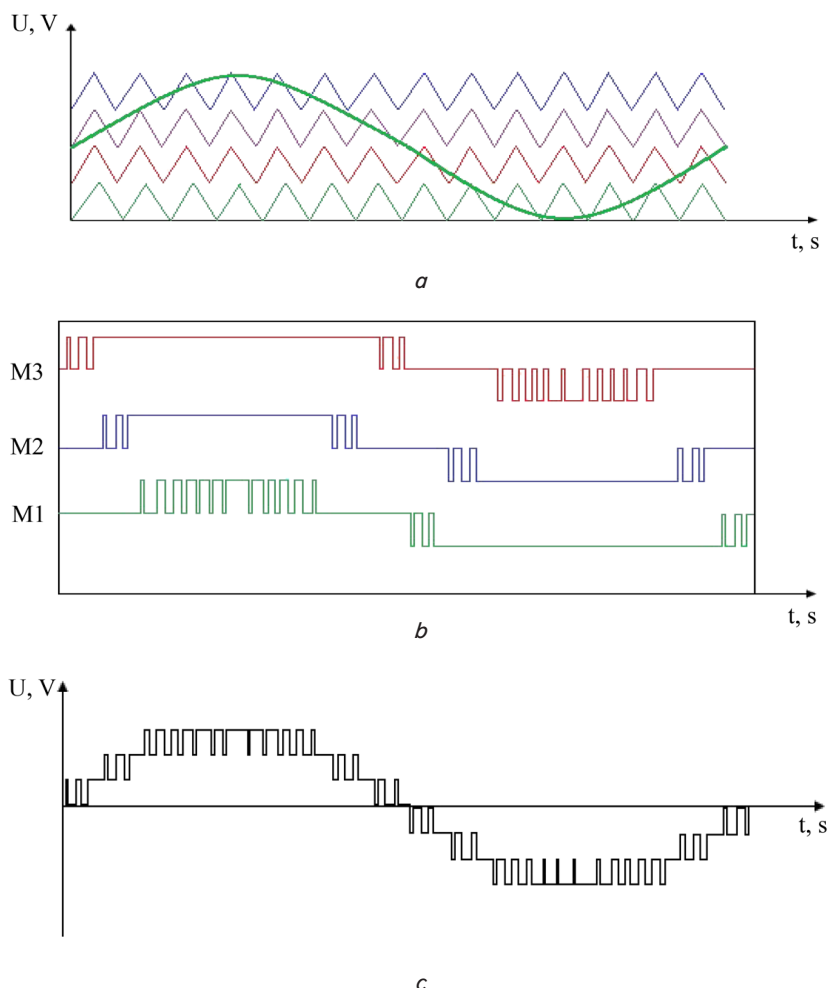


Fig. 2. Characteristics of a multi-level inverter with a level offset of carrier signals: *a* – modulating and carrier signals; *b* – control signals; *c* – output voltage

Phase shifted pulse-width modulation (PSPWM) was developed to solve the problem of the uniform loading of modules. Two main variants of the distribution of carrier signals have been proposed. In the first method, there are two carrier signals for each module as in LSPWM, but each has an amplitude of MU_{DC} . The switching moment is also determined similarly to LSPWM. The frequency of the carrier signals exceeds the apparent switching frequency by M times ($f_{CAR}=Mf_{sw}$), and the phase is shifted by an angle of $360^\circ/M$ relative to each other. In the second method, each module has one carrier signal with an amplitude of $2MU_{DC}$: from $-MU_{DC}$ to MU_{DC} . The switching frequency is determined similarly to the first method $f_{CAR}=Mf_{sw}$. However, the reference signal is multiplied by -1 , switching moments are determined by comparing the carrier signal with both reference signals. There is a noticeable difference between the two PSPWM methods under consideration. Although the frequencies of the carrier signal are equal, in the second method, key switching occurs twice as often as the first. The higher the switching frequency, the easier it is to maintain load balance between modules, but the disadvantage is an increase in switching losses.

To determine the dependence of the transition temperature on the installed capacity of the IGBT module, we will use the analytical dependence of the transition

temperature on the parameters of the power module, as well as the data obtained as a result of modeling. The installed power of the module is defined as the product of the average current value by the permissible voltage value. The table shows the values of the installed power of the bridge PWM inverter module operating on a load with a different power factor while maintaining the active load constant at the level of 100 kW.

Table 1

Values of current, voltage and power of the IGBT module when operating on a load with different power factors

| Power factor | 0.9 | 0.8 | 0.6 | 0.4 | 0.2 |
|--------------|--------|--------|--------|--------|---------|
| Current, A | 106 | 120 | 159 | 238 | 476 |
| Voltage, V | 363 | 363 | 363 | 363 | 363 |
| Power, kW | 38.478 | 43.560 | 57.717 | 86.394 | 173.264 |

The junction temperature of the module increases with the collector current, i.e. when installing a more powerful module with less thermal and electrical resistance, the junction temperature decreases. Thus, the transition temperature depends on the ratio of the output power of the module to its installed power. Let's call this ratio the load factor of the power module.

5. Research results of the analysis of power loss of multilevel inverters

5.1. The dependence of the total harmonic distortion on the frequency coefficient K_f for a different number of modules M

The two main characteristics affecting the harmonic composition of the voltage generated by multi-level PWM inverters are the number of inverter modules M (when considering the topology of a cascade bridge inverter, the number of series-connected bridge circuits) and the ratio of the frequency of the carrier signal to the frequency of the modulating K_f [18].

Spectral modeling can be used to find the distribution of harmonics in the output voltage spectrum. The modulating sinusoidal signal A does not depend on the serial number of the module m and is calculated according to the formula (3):

$$A_n = \sin(nd). \tag{3}$$

The output voltages of the modules O are determined by comparing the carrier and reference signals according to the formula (4):

$$O_{m,n} = \begin{cases} 1, & -A_n < r_{m,n} < A_n, \\ -1, & A_n < r_{m,n} < -A_n, \\ 0. & \end{cases} \tag{4}$$

The output voltage of the inverter V_n , determined by the algebraic sum of the output voltages of the modules, is calculated by the formula (5):

$$INV_n = \sum_{m=1}^M \left(\frac{E}{M} O_{m,n} \right) = \frac{E}{M} \sum_{m=1}^M O_{m,n}, \tag{5}$$

where E is the total voltage applied to the modules of the inverter.

Then the spectrum can be found by formula (6).

$$C_{\phi_k} = \sqrt{Cc\phi_k^2 + Cs\phi_k^2}, \tag{6}$$

where

$$Cc\phi_k = \frac{d}{\pi} \sum_n (INV_n \cdot \cos(n \cdot d \cdot k)), \tag{7}$$

$$Cs\phi_k = \frac{d}{\pi} \sum_n (INV_n \cdot \sin(n \cdot d \cdot k)). \tag{8}$$

Using the MathCad package, we calculate the inverter output voltage spectrum using the indicated formulas for various operating modes. The plots of the dependence of the total harmonic distortion THD on the specified characteristics obtained in this way are shown in Fig. 3. The graphs are obtained by approximating the values calculated for natural values of K_f , i.e. when an integer number of periods of the carrier signal is placed on one period of the modulating signal.

THD is a measure of the effective value of the harmonic components of a distorted waveform. This index can be calculated for either voltage or current:

$$THD = \frac{\sqrt{\sum_{h>0}^{h_{max}} M_n^2}}{M_1}, \tag{9}$$

where M_n is the RMS value of the harmonic component h of the quantity M .

Increasing the frequency of the carrier signal, as in the case of a single-level PWM, only leads to a shift of harmonics to the high frequency region, and does not remove them from the spectrum. Thus, the values of the total harmonic distortion, when calculating which harmonics up to and including the fortieth order are taken into account in accordance with requirements, decrease with increasing switching frequency. However, higher harmonics continue to have a negative impact on consumers. In contrast to the switching frequency, an increase in the number of modules leads to a decrease in the harmonic content in the spectrum of the voltage generated by the inverter, and not only an increase in their order.

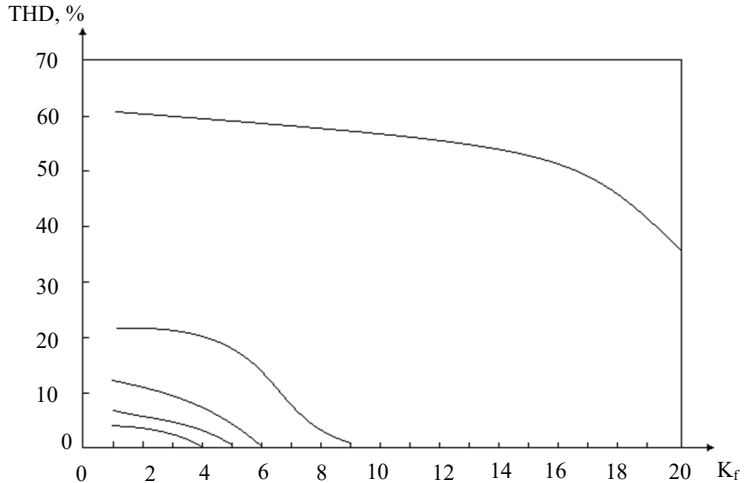


Fig. 3. Graph of total harmonic distortion versus frequency factor K_f

5.2. Analysis of power loss and transition temperature of power modules of a multilevel pulse-width modulation inverter

When modeling, we will not use voltage filters, even if the value of the total harmonic coefficient exceeds the accepted 8 %. This restriction is introduced due to the fact that when using a filter, even a single-level circuit provides a harmonic coefficient from 1 to 5 %, depending on the filter parameters. Thus, the use of a multi-level PWM inverter will require significantly higher hardware costs compared to PWM when powering the same load [19]. In such cases, the use of multi-level PWM can be justified either by too high values of the supply voltage and power, the values of which are not provided by one IGBT module and they are distributed between levels, or by the presence of a large number of low-voltage voltage sources, for example, when providing power from a network of wind generators or solar panels. In both cases, the use of a bridge circuit with PWM is impossible and there are no alternatives to an easily scalable PWM circuit.

To analyze the power loss and transition temperature of power modules of a multi-level PWM inverter, you can use the MATLAB/Simulink model, which is used to analyze single-level PWM inverters (Fig. 4).

The differences are in the models of the inverter itself and the control system. These models are shown in Fig. 5.

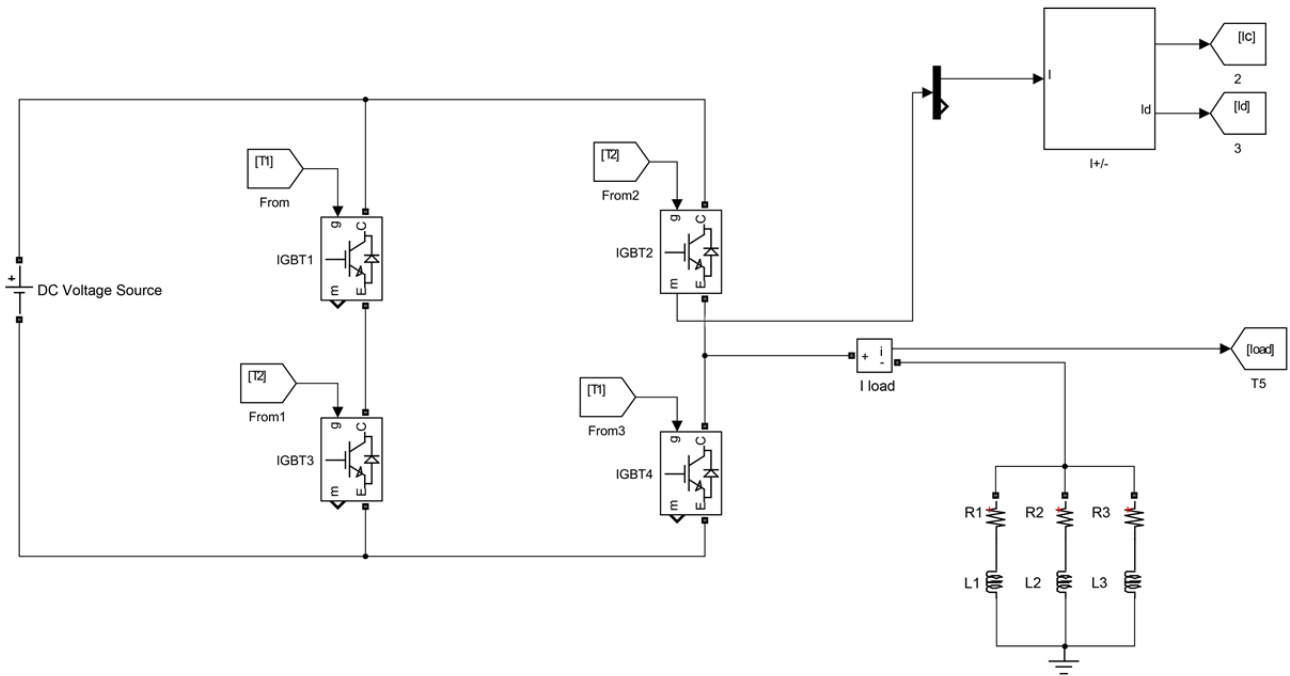


Fig. 4. Inverter model

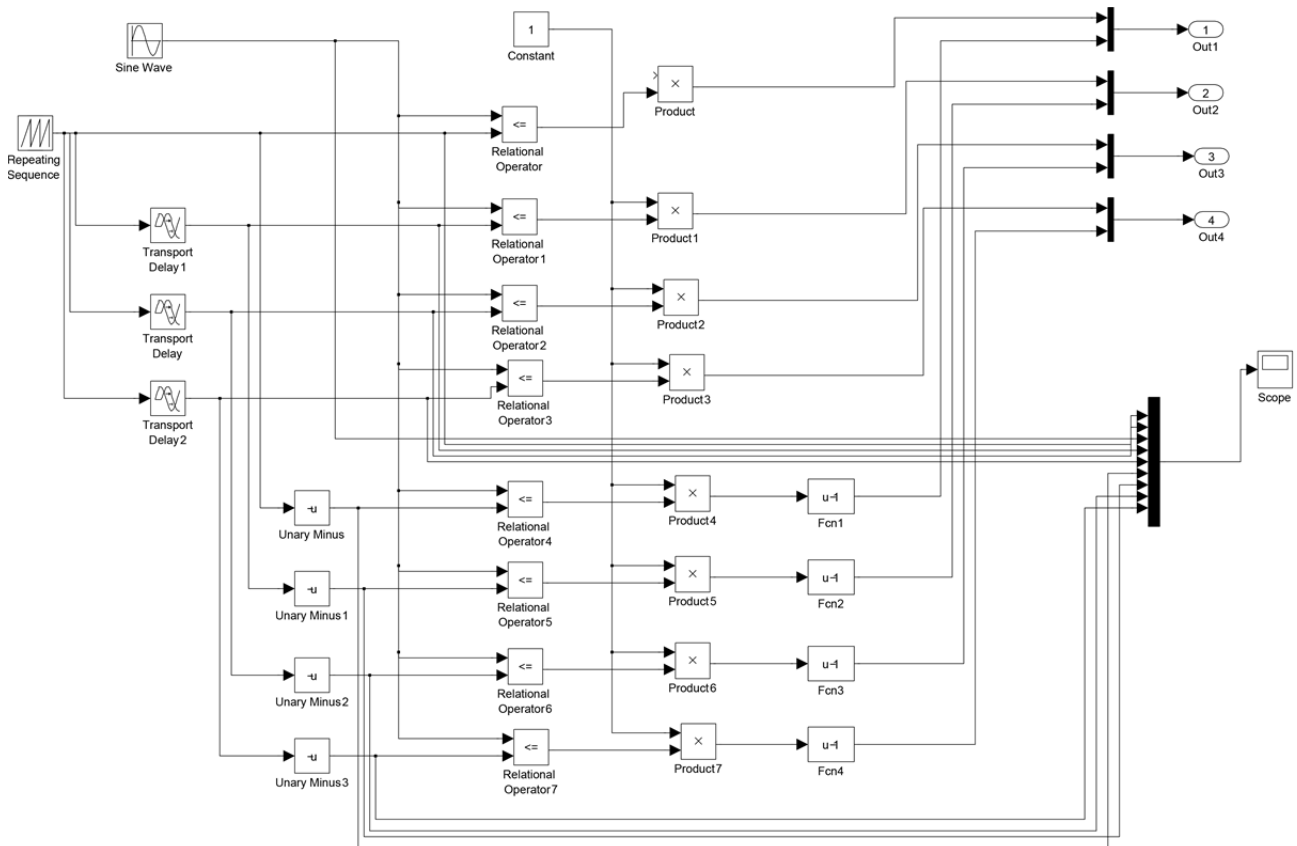


Fig. 5. MATLAB/Simulink – model of a control system for a 4-module cascade bridge inverter with a phase shift of carriers

For the inverter model, a cascade bridge topology is used, which has the property of scalability, i.e. increasing the number of output voltage levels without fundamentally changing the circuit itself. The control system of the model implements a multi-level PWM based on carrier signals with phase offset, which ensures uniform loading of all inverter bridges.

As a result of the simulation, the dependences of the transition temperature in IGBT modules of cascade PWM inverters on the switching frequency and the load power determining the collector current at different levels of the output voltage of the inverter were analyzed. The obtained dependences for a 5-level inverter at a cooling intensity of $R_{thSA}=0.1 \text{ }^\circ\text{C/Watts}$ for different load currents are shown in Fig. 6, 7. It can be seen from

the graphs that at a frequency below 8 kHz, the temperature depends mainly on the power output. The dynamic component of the losses is small and has little effect on the total losses in the module. However, at frequencies of 8–16 kHz, dynamic losses begin to have a noticeable effect on the total power loss and, consequently, the transition temperature.

When determining the temperature of the module, the following characteristics are used:

- the thermal resistance of the junction-housing R_{ThJC} , which determines the temperature difference between the junction and the housing and is measured in $^{\circ}C/W$;
- the thermal resistance of the cooler housing R_{SA} , which determines the temperature difference between the housing and the cooling radiator of the module ($^{\circ}C/W$);
- the thermal resistance of the cooler-environment R_{SA} , which determines the temperature difference between the cooling radiator and the environment ($^{\circ}C/W$).

The value of Z_{ThJC} can be determined from the family of graphs presented in the passport data based on the pulse duration and the duty cycle of the signal.

The R_{SA} value depends on the selected type of cooling: natural, forced air, water – as well as its intensity.

In mathematical representation

$$T_J - T_C = P_{SUM} \times Z_{thJC}(t_p).$$

$$T_C - T_S = P_{SUM} \times R_{CS}.$$

$$T_S - T_A = P_{SUM} \times R_{SA}.$$

After transformations and substitutions, we get the expression

$$T_J - T_A = P_{SUM} \times (Z_{thJC} + R_{CS} + R_{SA}).$$

The ambient temperature is considered constant and is usually assumed to be $40^{\circ}C$. The values of the thermal resistances of the junction-housing and the cooler housing are determined by the design of the module and are also constant. Thus, it is possible to reduce the transition temperature only by increasing the cooling intensity, i.e. reducing the value of the thermal resistance of the cooler-environment.

Knowing the values of the thermal resistance R_{SA} for various coolers, you can choose the type and intensity of the required IGBT cooling. It should be noted that as a result of the calculation, the R_{SA} value may turn out to be negative, which will indicate that it is impossible to use the selected IGBT module for these modulation and load parameters.

The obtained dependencies are valid for different modules and do not depend on the number of levels of the inverter. When operating on a constant load requiring a constant value of the supply voltage, an increase in the number of modules in a multi-level inverter entails a proportional decrease in the supply voltage of each module. So in our case, in order to provide an active power of 50 kW, necessary for comparison with PWM and PAM inverters, the total voltage of the supply elements should be 570 V. Thus, for a two-level inverter, a voltage of 285 V is applied to each bridge, for a three-level – 190 V, for a 4-level 142 V, for a five-level 114 V.

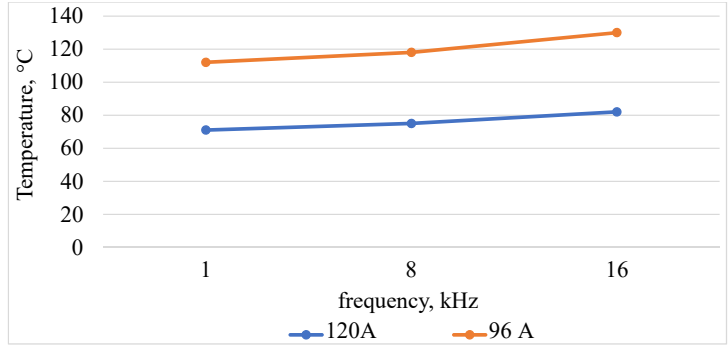


Fig. 6. Dependence of the transition temperature on the switching frequency for pulse-width modulation inverter

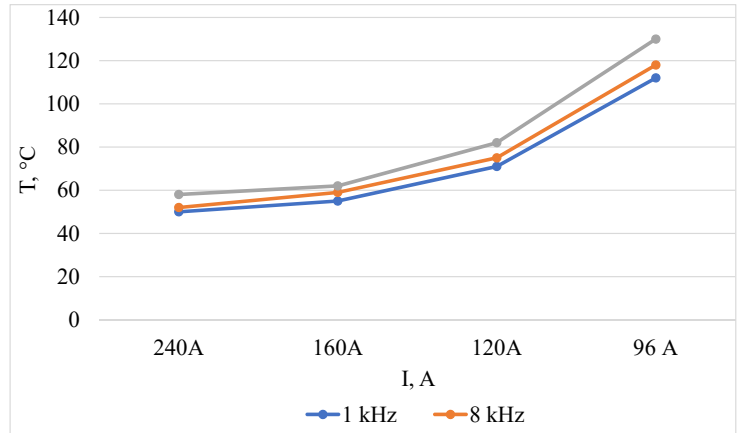


Fig. 7. Dependence of the transition temperature on the load power for pulse-width modulation inverter

The simulation results of the junction temperature presented in Table 2 show that the junction temperature, despite the voltage decrease, turns out to be unchanged.

Table 2

Transition temperature of IGBT modules of a multilevel inverter depending on the switching frequency and the number of output voltage levels when operating on the same load

| Frequency of carrier signal, kHz | Number of output voltage levels per quarter period | | | |
|----------------------------------|--|------------------|------------------|------------------|
| | 2 | 3 | 4 | 5 |
| 1 | 130 ⁰ | 131 ⁰ | 132 ⁰ | 129 ⁰ |
| 2 | 129 ⁰ | 130 ⁰ | 126 ⁰ | 128 ⁰ |
| 4 | 135 ⁰ | 136 ⁰ | 136 ⁰ | 136 ⁰ |
| 8 | 147 ⁰ | 147 ⁰ | 148 ⁰ | 146 ⁰ |
| 16 | 166 ⁰ | 167 ⁰ | 169 ⁰ | 165 ⁰ |

This means that the temperature increases linearly with increasing switching frequency, but remains unchanged at different levels of supply voltage. This is explained by the fact that the total voltage, and with it the collector current, remain unchanged, therefore, the values of static and dynamic power losses remain unchanged.

5.3. Simulation of a high-frequency inverter with smooth switching

A high-frequency inverter with smooth switching with phase shift and a step-up converter is modeled. Another

stage of the inverter is switching the inverter cascade with a PS-PWM control circuit. Along with the growing demand for high-power density conversion, IGBT transistors are preferred over field-effect MOSFETs in applications with a large power range [20]. IGBT transistors are designed for higher rated voltages and currents. Additionally, these transistors have lower conduction losses compared to MOSFETs. However, IGBT is slower than MOSFET (IGBT frequency is usually limited to 20–30 kHz) due to higher switching losses resulting from the tail current at shutdown. Therefore, if an IGBT transistor is to be used for higher switching frequencies, the switching loss should be minimized. The solution can be either switching at zero voltage (ZV), which is carried out by adding an external snubber capacitor or switching at zero current (ZC). Switching at zero current seems to be more efficient than switching at zero voltage, since the tail current problem can be eliminated to a minimum by removing the non-main carriers before switching off.

The study [21] mainly contributes to the creation of an applicable methodology with detailed information for obtaining average switching power losses using the selected switching loss model. This method works properly when the switched current or switched voltage is an alternative.

An experimental study of the operation of a multi-stage three-phase half-bridge inverter was carried out in the Matlab engineering program, in the Simulink section. The circuit consists of three DC voltage sources (DC1, DC2, DC3), 12 transistors, three loads (Fig. 8).

The main transistors (T1, T2, T3, T4, T5, T6) are controlled through a Subsystem2 control unit consisting of 6 pulse generators that transmit control signals in the form of pulses to the transistor base. Transistors T7, T8 and T9 serve to form stages of a positive half-cycle of the output voltage at the load. Its control unit is Subsystem1, which also consists of pulse generators. Transistors T10, T11 and T12 serve to form stages of a negative half-cycle of the output

voltage on the load, its control unit is Subsystem2. Voltmeters take readings on loads and display their graph on an oscilloscope. The operation algorithm of transistors is shown in Fig. 9.

For the convenience of the study, we divide the total field into cells, each “cell” is equal to 200. Next we have 12 lines. Each line is the operating time of each individual transistor. The data on the graph is given in degrees, but for convenience they can be translated into seconds (Table 3).

Table 3

The algorithm of transistors

| Transistor number | Opening | | Closing | |
|-------------------|------------|------------|------------|------------|
| | In degrees | In seconds | In degrees | In seconds |
| Transistor 1 | 0° | 0.00 | 180° | 0.01 |
| Transistor 2 | 180° | 0.01 | 360° | 0.02 |
| Transistor 3 | 120° | 0.006667 | 300° | 0.016667 |
| Transistor 4 | -60° | -0.003333 | 120° | 0.006667 |
| Transistor 5 | -120° | -0.006667 | 60° | 0.003333 |
| Transistor 6 | 60° | 0.003333 | 240° | 0.013333 |
| Transistor 7 | 20° | 0.001111 | 160° | 0.008889 |
| Transistor 8 | 140° | 0.007778 | 280° | 0.015556 |
| Transistor 9 | -100° | -0.005556 | 40° | 0.002222 |
| Transistor 10 | 200° | 0.011111 | 340° | 0.018888 |
| Transistor 11 | -40° | -0.002223 | 100° | 0.005555 |
| Transistor 12 | 80° | 0.004443 | 220° | 0.012221 |

Pulse generators that were used to control transistors, the switching phase is set by the “time” parameter. And for this, all the degrees of opening were converted into seconds. The total frequency of our output voltages is 50 Hz.

The output voltages describe a sine, and have a difference of 120° degrees. The waveform at the output of the inverter is shown in Fig. 10.

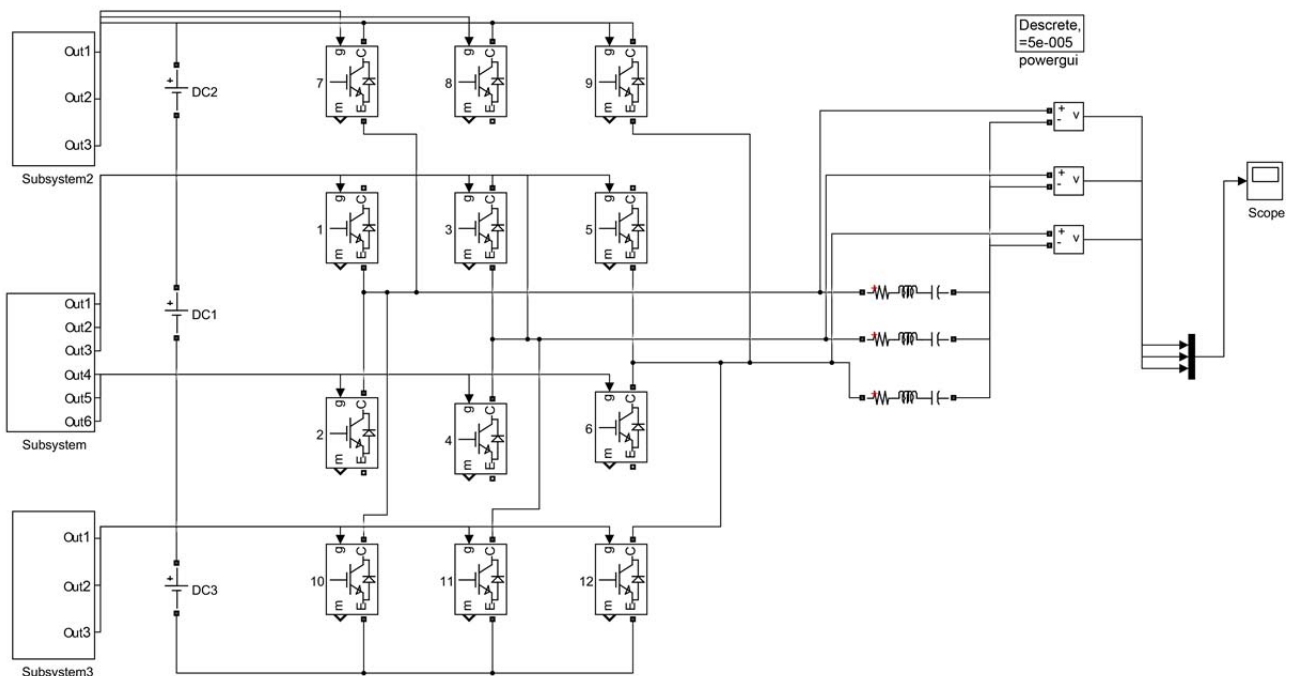


Fig. 8. Basic structure of a bridge single-phase voltage inverter in the Simulink/ Matlab software environment

The results of the spectral analysis show the presence of amplitudes at the 5th, 17th and 19th harmonics (Fig. 11).

But their amplitudes do not reach even 5 percent of the first harmonic. Then they can be eliminated by filters without experiencing large output voltage losses.

A 6 kW three-phase inverter with a control system was developed and manufactured, which is shown in Fig. 12. In addition, the three-phase inverter was tested offline in the “Battery – converter – three-phase inverter – load” system, which is shown in Fig. 13.

| | | |
|-----------------|--------|--------|
| 0 Hz (DC) : | 0.14 | 90.0° |
| 50 Hz (Fnd) : | 311.80 | 0.0° |
| 100 Hz (h2) : | 0.28 | 90.0° |
| 150 Hz (h3) : | 1.31 | 137.0° |
| 200 Hz (h4) : | 0.28 | 90.0° |
| 250 Hz (h5) : | 13.63 | 0.0° |
| 300 Hz (h6) : | 0.28 | 90.0° |
| 350 Hz (h7) : | 8.64 | 168.1° |
| 400 Hz (h8) : | 0.28 | 90.0° |
| 450 Hz (h9) : | 0.85 | 85.8° |
| 500 Hz (h10) : | 0.28 | 90.0° |
| 550 Hz (h11) : | 5.04 | 160.4° |
| 600 Hz (h12) : | 0.28 | 90.0° |
| 650 Hz (h13) : | 5.88 | 0.0° |
| 700 Hz (h14) : | 0.28 | 90.0° |
| 750 Hz (h15) : | 1.22 | 30.0° |
| 800 Hz (h16) : | 0.28 | 90.0° |
| 850 Hz (h17) : | 17.91 | 0.0° |
| 900 Hz (h18) : | 0.28 | 90.0° |
| 950 Hz (h19) : | 16.66 | 0.0° |
| 1000 Hz (h20) : | 0.28 | 90.0° |
| 1050 Hz (h21) : | 1.39 | 124.4° |
| 1100 Hz (h22) : | 0.28 | 90.0° |
| 1150 Hz (h23) : | 2.57 | 0.0° |
| 1200 Hz (h24) : | 0.28 | 90.0° |
| 1250 Hz (h25) : | 2.88 | 140.8° |
| 1300 Hz (h26) : | 0.28 | 90.0° |
| 1350 Hz (h27) : | 0.84 | 77.4° |
| 1400 Hz (h28) : | 0.28 | 90.0° |
| 1450 Hz (h29) : | 1.98 | 129.4° |
| 1500 Hz (h30) : | 0.28 | 90.0° |
| 1550 Hz (h31) : | 2.68 | 0.0° |
| 1600 Hz (h32) : | 0.28 | 90.0° |
| 1650 Hz (h33) : | 1.13 | 16.4° |
| 1700 Hz (h34) : | 0.28 | 90.0° |
| 1750 Hz (h35) : | 8.42 | 0.0° |
| 1800 Hz (h36) : | 0.28 | 90.0° |
| 1850 Hz (h37) : | 8.62 | 0.0° |
| 1900 Hz (h38) : | 0.28 | 90.0° |
| 1950 Hz (h39) : | 1.47 | 111.9° |

Fig. 11. Results of spectral analysis

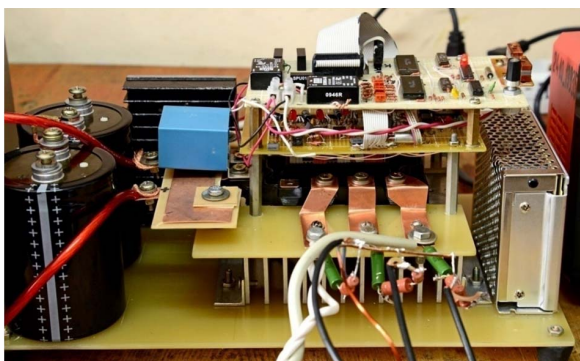


Fig. 12. Three-phase inverter with a control system



Fig. 13. Test scheme for the system “Battery – converter – three-phase inverter – load”

According to the test results, the three-phase inverter was brought to a stable state, in which a phase shift between phase voltages of 120 degrees with a frequency of 50 Hz was provided at the output of the inverter. An oscillogram of phase voltages providing a phase shift of 120 degrees with a frequency of 50 Hz is shown in Fig. 14.



Fig. 14. Waveform of phase voltages of a three-phase inverter

The test results showed that the three-phase inverter works stably and requires an improvement in the shape of the output voltage curve.

6. Discussion of the results of research on power losses of multilevel inverters

Comparing the different types of modern frequency converters, it is possible to identify the main features inherent in all circuits:

- the switching elements used are mainly high-power bipolar transistors with an isolated gate – IGBT, as well as field-effect MOSFET transistors;
- building a microcontroller-based control system.

Comparing studies between different levels of cascaded multi-level H-bridge inverters, the choice should be based on the topology of each inverter, which is to use an inverter. Each topology has its advantages and disadvantages. With an increase in the number of THD levels, the cost will be reduced, on the other hand, it will also be overweight (Fig. 3). The cascade multilevel inverter topology of the H-bridge requires only one DC power supply. Taking into account certain limitations, it was shown that the level of voltage capacitors can be controlled by choosing the angles of si-

multaneous shift to achieve a certain modulation index and reduce harmonics in the form of an output wave.

The process of calculating dynamic losses is complicated by the nonlinear form of current and voltage in the transistor at the time of its switching on and off. The values change very quickly, which makes it impossible to carry out a simple simulation of this process or an analytical calculation. Therefore, for the analysis of dynamic losses, the values of the energy of switching on and off the transistor obtained on a special test bench and given in the IGBT module passport are used. The on- and off-energy determine the amount of energy dissipated on the transistor in one cycle of switching on and off, respectively. Since, when calculating the power losses, the total power for the period of the modeling signal or for the clock of the carrier signal is of interest, and the on-off time of the transistor is 10^{-8} – 10^{-9} s, then the on/off losses can be represented as single pulses, the amplitude of which is equal to the value of the on/off energy.

The power loss affects the transition temperature, denoted T_j , the maximum allowable value of which for most modules is 126–169 °C. The transition temperature is determined by the power loss in the IGBT module, the intensity of its cooling, the ambient temperature, as well as the design characteristics that determine thermal resistance, i.e. heat transfer from the module to the environment (Table 2).

Soft switching circuits connected to the inverter AC circuit are largely devoid of the disadvantages that were noted in previous solutions. The peculiarity of these circuits is that the switching choke in them is removed from the operating current circuit of the converter, and the operation of auxiliary transistors is pulsed. The capacitor C_d at the input is a mandatory element (Fig. 8). It has a twofold purpose: it provides constant consumption from the power source even when the keys are in a forbidden state and protects semiconductor elements from over-voltages that occur on the connecting wires between the power source and the valve block.

The basic scheme of a bridge single-phase voltage inverter based on the control structure. The essence of controlling a single-phase bridge inverter is that switching transistors in the circuit occurs at a time when the voltage passes through zero. Due to this, it is possible to achieve a reduction in switching losses.

The operation principle of the inverter is based on changing the structure of the step-up DC-DC capacitor converter, alternating switching of transistor switches VT3, VT4 with a frequency of 50 Hz. In this case, there is an abrupt change in the conversion coefficient for the study, leading

to a change in the output voltage U_{out} . By the influence of harmonic PWM on the transistors of the VTM bridge, we obtain a sinusoidal current in the load I_{Ld} . An important advantage of the inverter in question is the reduced dynamic voltage drop on the bridge transistors not exceeding in the system in question.

This makes it possible to further increase the inverter efficiency by 1.5–2 % by reducing power losses for switching losses in the bridge transistors. The disadvantage of the inverter in question is the pulsating current consumed from the battery. The value of current ripples I is twice the current ripple in the load, which negatively affects the battery operation.

7. Conclusions

1. The influence of frequency carrier signal on harmonic distortion in multilevel inverters was investigated. The analysis concerns the performance characteristics of the inverter using common PWM strategies for different values of carrier frequency and modulation index. In addition, there are implementation problems and some practical considerations for optimizing implementation and reducing computational costs. At the same time, an increase in the number of levels has a positive effect on reducing the harmonic content in the voltage spectrum, while an increase in frequency only shifts the harmonic groups higher in the spectrum.

2. It is proved that when using multi-level PWM inverters, increasing the number of levels reduces the installed power of each of their modules, but does not affect the transition temperature. Based on this, the use of multi-level PWM inverters with a large number of modules is justified only in two cases:

- the value of the supply voltage exceeds the rated voltage of IGBT modules, which for most modules is 1200–2500 V. This is relevant for the construction of high-voltage frequency converters;

- the required harmonic composition of the output voltage does not allow the use of an inverter with a small number of levels without the use of a filter.

3. A computer simulation of a bridge voltage inverter based on a control structure based on IGBT transistors was performed, volt-ampere characteristics were obtained, a detailed analysis was carried out. The analysis of electrical processes is carried out, which allows calculating the parameters of the operating modes of the elements of the power circuit and giving recommendations for use in converters.

References

1. Garapati, D. P., Nalli, P. K., Swaroop, K. P., Vijay Kumar, Y. (2021). She-Pwm Low Cost Multi Level Inverter for Pv Based Water Pumping Applications. *Journal of Physics: Conference Series*, 2089 (1), 012019. doi: <https://doi.org/10.1088/1742-6596/2089/1/012019>
2. Dahidah, M. S. A., Agelidis, V. G. (2008). Selective Harmonic Elimination PWM Control for Cascaded Multilevel Voltage Source Converters: A Generalized Formula. *IEEE Transactions on Power Electronics*, 23 (4), 1620–1630. doi: <https://doi.org/10.1109/tpe.2008.925179>
3. Prasad, G. D., Jegathesan, V., Rao, P. V. V. R. (2017). Hybrid multilevel DC link inverter with reduced power electronic switches. *Energy Procedia*, 117, 626–634. doi: <https://doi.org/10.1016/j.egypro.2017.05.162>
4. Ketjoy, N., Chamsa-ard, W., Mensin, P. (2021). Analysis of factors affecting efficiency of inverters: Case study grid-connected PV systems in lower northern region of Thailand. *Energy Reports*, 7, 3857–3868. doi: <https://doi.org/10.1016/j.egy.2021.06.075>
5. Kanike, V. K., Raju, S. (2020). Analysis of Switching Sequence Operation for Reduced Switch Multilevel Inverter With Various Pulse Width Modulation Methods. *Frontiers in Energy Research*, 7. doi: <https://doi.org/10.3389/fenrg.2019.00164>

6. Shema, S. S., Daut, I., Irwanto, M., Shatri, C., Syafawati, N., Ashbahani, N. (2011). Study of inverter design and topologies for photovoltaic system. International Conference on Electrical, Control and Computer Engineering 2011 (InECCE). doi: <https://doi.org/10.1109/inecce.2011.5953934>
7. Zhao, D., Yang, L., Wang, L., Wang, Q. (2015). Research on the inverter circuit of power generation system. 2015 IEEE 5th International Conference on Electronics Information and Emergency Communication. doi: <https://doi.org/10.1109/iceiec.2015.7284571>
8. Farooqui, S. A., Shees, M. M., Alsharekh, M. F., Alyahya, S., Khan, R. A., Sarwar, A. et. al. (2021). Crystal Structure Algorithm (CryStAl) Based Selective Harmonic Elimination Modulation in a Cascaded H-Bridge Multilevel Inverter. *Electronics*, 10 (24), 3070. doi: <https://doi.org/10.3390/electronics10243070>
9. Dhineshkumar, K., Subramani, C., Geetha, A., Vimala, C. (2019). Performance analysis of PV powered multilevel inverter. *International Journal of Electrical and Computer Engineering (IJECE)*, 9 (2), 753. doi: <https://doi.org/10.11591/ijece.v9i2.pp753-760>
10. Maaroo, H. S., Al-Badrani, H., Younis, A. T. (2021). Design and simulation of cascaded H-bridge 5-level inverter for grid connection system based on multi-carrier PWM technique. *IOP Conference Series: Materials Science and Engineering*, 1152 (1), 012034. doi: <https://doi.org/10.1088/1757-899x/1152/1/012034>
11. Al-Modaffer, A. M., Chlahawi, A. A., Wahhab, H. A. (2020). Non-isolated multiple input multilevel output DC-DC converter for hybrid power system. *Indonesian Journal of Electrical Engineering and Computer Science*, 19 (2), 635. doi: <https://doi.org/10.11591/ijeecs.v19.i2.pp635-643>
12. Babkrani, Y., Naddami, A., Hilal, M. (2019). A smart cascaded H-bridge multilevel inverter with an optimized modulation techniques increasing the quality and reducing harmonics. *International Journal of Power Electronics and Drive Systems (IJPEDS)*, 10 (4), 1852. doi: <https://doi.org/10.11591/ijpeds.v10.i4.pp1852-1862>
13. Seifi, A., Hosseinpour, M., Dejamkhooy, A., Sedaghati, F. (2020). Novel Reduced Switch-Count Structure for Symmetric/Asymmetric Cascaded Multilevel Inverter. *Arabian Journal for Science and Engineering*, 45 (8), 6687–6700. doi: <https://doi.org/10.1007/s13369-020-04659-4>
14. Sathik, M. J., Almakhles, D. J., Sandeep, N., Siddique, M. D. (2021). Experimental validation of new self-voltage balanced 9L-ANPC inverter for photovoltaic applications. *Scientific Reports*, 11 (1). doi: <https://doi.org/10.1038/s41598-021-84531-z>
15. Lee, S. S., Siwakoti, Y., Barzegarkhoo, R., Lee, K.-B. (2021). Switched-Capacitor-Based Five-Level T-Type Inverter (SC-5TI) With Soft-Charging and Enhanced DC-Link Voltage Utilization. *IEEE Transactions on Power Electronics*, 36 (12), 13958–13967. doi: <https://doi.org/10.1109/tpel.2021.3088443>
16. Lysenko, O. A., Okhotnikov, A. A., Zakharenko, V. A., Kobenko, V. Y. (2019). The study of five-level inverters with various PWM. *Omsk Scientific Bulletin*, 168, 34–39. doi: <https://doi.org/10.25206/1813-8225-2019-168-34-39>
17. Antar, R. K., Saied, B. M., Khalil, R. A. (2012). Using seven-level cascade H-bridge inverter with HVDC system to improve power quality. 2012 First National Conference for Engineering Sciences (FNCES 2012). doi: <https://doi.org/10.1109/nces.2012.6740457>
18. Shcherbakov, A. A. (2011). Spectral modeling of multilevel voltage inverters. *Problems of electric power industry*, 141–145.
19. Bouzida, A., Abdelli, R., Ouadah, M. (2016). Calculation of IGBT power losses and junction temperature in inverter drive. 2016 8th International Conference on Modelling, Identification and Control (ICMIC). doi: <https://doi.org/10.1109/icmic.2016.7804216>
20. Zotov, L. G., Breido, J. V., Isembergenov, N. T., Yugay, V. V. (2015). Methods for Controlling Autonomous DC System on the Basis of Switching by Capacitors. *Modern Applied Science*, 9 (4). doi: <https://doi.org/10.5539/mas.v9n4p135>
21. Hasari, S. A. S., Salemnia, A., Hamzeh, M. (2017). Applicable Method for Average Switching Loss Calculation in Power Electronic Converters. *Journal of Power Electronics*, 17 (4), 1097–1108. doi: <https://doi.org/10.6113/JPE.2017.17.4.1097>