The compact switched-capacitor converter with exponential gain and modular design has been adopted in this paper. Two approaches have been applied to improve the efficiency by providing multiple no-load voltages. The first modifies the switching strategy to bypass the gain of one or more stages. The second introduces modified design that provide additional no-load voltages through alternative current paths. The voltage regulation is implemented by two control loops: The outer loop is designed to produce the minimum feasible no-load voltage and the inner loop adjusts the duty ratio of the switching signals to regulate the voltage to meet the desired reference. Switched capacitor converters have been used as voltage multipliers with constant voltage gain. The efficiency of a switched capacitor converter depends on the ratio between regulated to unregulated output voltage. Therefore, output voltage adjustment of these converters causes a significant efficiency reduction. By providing multiple no-load voltages within the output voltage range the efficiency of the switched capacitor converter can be improved. The proposed design has been applied to a three-stage converter to provide six no-load voltages. Simulation results demonstrate that the average efficiency over the entire output voltage range is more than 90 % of its maximum efficiency of the unregulated switched capacitor converter which reflects the effectiveness of the proposed scheme. This paper offers an efficient method to regulate the voltage of a modular switched capacitor converter with exponential gain. The advantages of the proposed design are small number of added components, does not require additional sources and suitable for higher power range

Keywords: DC-DC converter, switched capacitor, power conditioning, inductor-less converter, voltage multiplier

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DEVELOPMENT OF AN EFFICIENT VOLTAGE REGULATION MECHANISM FOR SWITCHED CAPACITOR CONVERTER WITH EXPONENTIAL GAIN

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1. Introduction

Step-up DC-DC converters with high voltage gain and wide voltage range are required in variety of applications [1, 2]. Most step-up converters use inductors to trap energy in order to lift the output potential [3–5]. Switched Capacitor Converter (SCC) provides an alternative approach by using capacitors and switches only [6]. Due to the fact that typical integrated inductors are not yet adequate for power electronic applications, SCCs are the best choice for integrated implementations. SCCs can enable a higher power density compared to conventional converters for a given conversion ratio, despite the fact that they can only support a limited number of conversion ratios. Therefore, the SCCs have recently attracted attention in industry and research for their attractive features such as lightweight, tolerance to operate in high temperature; suitability for fabrication as integrated circuits and reduced electromagnetic interference (EMI). The main drawbacks of SCC, however, are the need for a large number of switching devices and incompetency to provide adjustable gain [7–9].

Voltage gain adjustment is crucial for many applications such as consumer electronics and medical equipment supplies. With SCC, the adjustment leads to efficiency reduction. Addressing this problem led to special designs with considerable increase in number of capacitor and switches and more control complexity. Therefore, it is important to develop a SCC with the feature of efficient voltage control and without many added components.

2. Literature review and problem statement

The paper [10] presented a modulation method to enhance the efficiency of a SCC operates to supply portable electronic devices assuming a wide range of load variation. It has been shown that decreasing the pulses frequency at light loading cuts the frequency-dependent losses and there-

fore enhances the efficiency. A special pulse frequency modulation was applied. This approach is not applicable for higher power ranges where this type of losses is not significant.

In the paper [11], a 3X flying-capacitor SCC is designed as a high-power converter. The converter operates at a constant frequency and intended to step-up the input voltage. In this design, the maximum gain is limited as the gain equals to the number of switches in the current path. Other designs have been suggested to overcome this limitation. For instance, the Modular Multilevel Clamped Capacitor Converter (MMCCC) has been designed with three series switches current path regardless of the gain [12]. In this design, however, the switches and capacitors are rated at the output voltage level. The high voltage rating required for the components is the drawback of the MMCCC. In [13] the multi-arm bridge was introduced to charge two series capacitors in each converter stage. The new converter has smaller capacitors rating and number of components -to-gain ratio. This design, as for the two preceding converters described in papers [11, 12], has unregulated gain.

The paper [14] presented a design of SCC with adjustable gain. In this work a 3x switched capacitor voltage multiplier is added as an output stage to a boost converter. The voltage gain is controlled by adjusting the duty ratio of the boost stage switch. High gain has been obtained while maintain high efficiency. By using inductor, this design spoils the advantages sought from SC converter.

In paper [15], output voltage regulation of a SCC was achieved by controlling the switching frequency. It has been shown through the theoretical analysis that output resistance of the SCC is frequency dependent and adjusting this frequency has the effect of changing the output resistance and, therefore, the output voltage. This control, however, directly effects the converter efficiency and is could be considered only for low power and non-portable applications.

One approach to achieve voltage regulation efficiently is based on designing a converter with multiple open-circuit voltages. In the design described in [16], it is shown that the four-capacitor converter can provide up to 21 no-load voltages in the step-down SCC. The implementation of this concept is based on establishing multiple circuit configurations (phases) within the switching cycle which requires full flexibility in the connection of capacitors. The design, therefore, is not suitable for high power circuits due to the large number of switches required.

For higher power converters, two-phase operation cycle and small number of switches are essential. In the paper [17], a converter with 11 output voltage levels has been assembled using two sources and basic SCC circuits. This approach depends on the availability of multiple supplies, which leads to additional cost and degraded reliability.

The paper [18] presented a multiple output voltage SCC based on Dickson converter. The 8 capacitors converter has 4 values of the gain in each of step-up and step-down modes. In this design, the switching signals determine the active path and therefore the converter gain. The design, however, applies large number of components, where the implemented circuit has 8 capacitors and 4 values of the gain in each of step-up and step-down modes. The paper [19] presented another design approach that use multi-section SCC that can be reconfigured using low frequency logic-driven switches. The bidirectional cascaded ladder SCC produces 5 levels in step-up and step-down modes by altering the connection points of the cascaded sections. The multiple section designs have an added circuitry and consequently large components count.

Consequently, the concentration of this work is to effectively obtain adjustable voltage gain of an inductor less SCC. To extend the voltage range, it is essential to provide multiple uncontrolled gain values by additional circuit components. This works deals with this problem to provide a design with minimum number of added components.

3. The aim and objectives of the study

The aim of this study is to efficiently control the output voltage over a wide range of a SCC based on the design known as the Compact Modular Switched Capacitor Converter (CMSCC) presented in [20]. This will make it possible to extend the applications of this topology as variable voltage power supply for electronic equipment.

To achieve this aim, the following objectives are accomplished:

– imposing voltage regulation by duty cycle adjustment of the basic CMSCC using a PI voltage controller;

– efficiency enhancement by adding no-load voltage levels using both switching signals modification and introducing the MCMC design for this purpose with the corresponding control.

4. Materials and methods of research

4. 1. Object and hypothesis of the study

Voltage regulation of an SCC can be achieved by frequency control [10]. Reducing the switching frequency allows the capacitors voltage to drop and accordingly decreases the output voltage. In this study an equivalent effect on the output voltage has been achieved by reducing the duty ratio, i.e., the ratio of the capacitor energization interval to the total switching time. Anyhow, voltage regulation reduces the converter efficiency nearly to the ratio of regulated-to-unregulated voltages. This work provides multiple values of the unregulated output voltages and controls the converter to produce the desired voltage at maximum possible efficiency.

The CMSCC adopted in this work, is composed of similar cascaded stages each stage doubles the voltage. By idling one stage, the converter gain can be halved. Therefore, this method can provide additional unregulated voltages. However, this method is not sufficient mainly because it gives only limited number of unevenly spaced voltages. In the suggested MCMC, limited number of switches have been added to allow a capacitor in a subsequent stage to be convert a voltage provided in a preceding stage. Additional values of unregulated voltages with more even distribution over the entire voltage range can be obtained.

Because the study aims applications in higher power range compared to other regulated SCC, the switching devices gate power has been ignored. Besides that, as the switching frequency is fixed, the parasitic inductance of the conductors has not been taken into account.

The study depends on simulation tool to obtain the converter output resistance, no analysis to derive this resistance has been included.

4. 2. Converter circuit and switching signals.

The nominal efficiency of SCC converter can be represented as follows [16]:

$$\eta_{c,nom} = \frac{V_o}{V_{o,oc}}, \quad (1)$$

where $V_{o,oc}$ is the open circuit (no-load) voltage. To maintain high efficiency, the output voltage, V_o, is required to be as close as possible to $V_{o,oc}$. The difference between V_o and $V_{o,oc}$ is due to the voltage drop across the output equivalent resistance (R_o).

$$V_o = V_{o,oc} - I_o R_o. \quad (2)$$

At low frequencies, R_o is inversely proportional to the switching frequency and independent on the switch on-state resistance. As the frequency exceeds the slow switching limit (SSL), the converter output resistance is determined by the switches on-state resistance and other parasitic resistors [19].

The CMSCC design has been developed to provide an output voltage that increases exponentially with the number of stages [20]. The unidirectional version of this converter is shown in Fig. 1, *a*. The basic converter has two operation phases: phase A and phase B. In phase A, switches $Q_{i,A}$ turn ON to charge the capacitors $C_{i,A}$. In phase B, switches $Q_{i,B}$ turn ON to charge the capacitors and $C_{i,B}$, where i=1,..n, where n represents the number of stages. Each stage doubles the voltage, consequently, the nominal gain ($V_{o,oc}/V_i$) is 2^n. The switching signals as proposed in [20] are shown in Fig. 1, b with a small blanking interval between the two phases. This switching method is applicable to all converter stages. It can be noted, however, that the switching signals are applicable as long as it satisfies the following condition:

$$\phi_{i,A} \wedge \phi_{i,B} = 0, \quad (3)$$

where $\phi_{i,A}$ and $\phi_{i,B}$ are the logic switching functions that drive the switching devices of the i^{th} stage; and $\wedge$ stands for the logic AND operator.

The stage-shifted switching signals can be applied to improve capacitor voltage balance, reduce input current ripple, and consequently reduce the losses. The shifted switching signals of the cascaded stages are displaced by $1/n$ of a cycle. For the 3-stage converter, the signals are shown in Fig. 1, *c*. In the following discussion, let'sl refer to the identical switching of various branches, shown in Fig. 1, *b* as common mode switching.

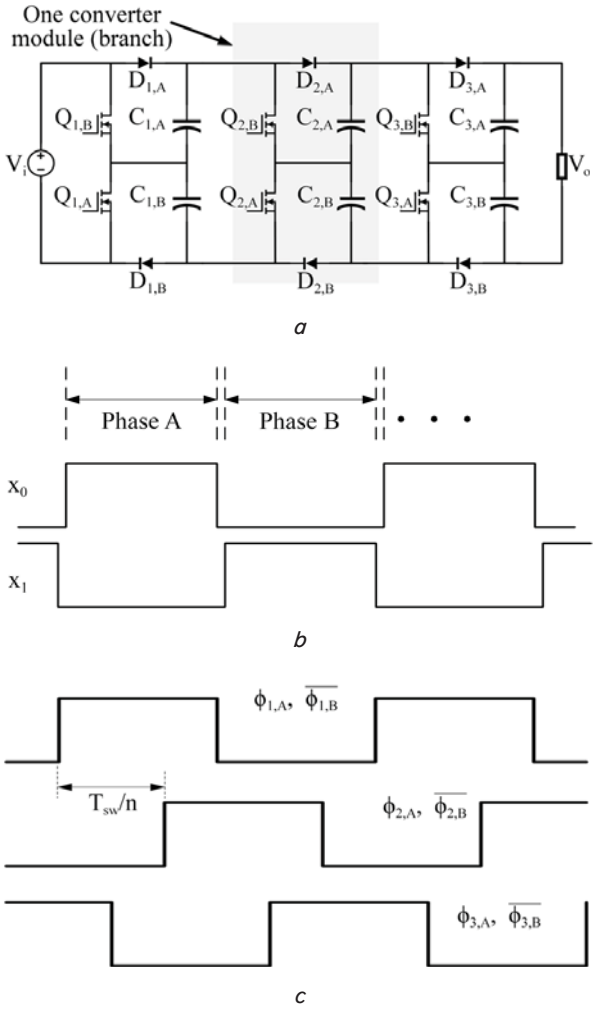

Fig. 1. Compact modular switched capacitor: *a* — circuit diagram; *b* — common mode switching signals; *c* — shifted switched signals

4. 3. Voltage control

Voltage regulation by duty ratio adjustment is described in the following subsection. Next, to enhance efficiency, the production of multiple no-load voltages is presented using two approaches: stage gain suppression and modified converter.

Considering the problem of voltage regulation of CMSCC shown in Fig. 1, *a*, the output voltage can be regulated by adjusting R_o. At switching frequencies below SLL R_o is inversely proportional to the switching frequency, therefore, the output voltage can be controlled by changing the switching frequency. Alternatively, decreasing the duty ratio of the switching devices also increase R_o. The two methods cause power losses proportional to the square of the voltage difference before and after regulation [8]. Accordingly, (1) represents the efficiency for both frequency and duty ratio control.

In this study, output voltage regulation has been implemented by duty ratio control. This method offers more flexibility than frequency control as it provides the option of controlling the gain of one stage or multiple stages. The flexibility can be exploited to reduce ripples of the input current and the load voltage. After assigning a switching frequency near the SSL, the converter gain can be varied from 1 to its maximum as the duty ratio of each switching signal changes from 0 to 0.5.

4. 4. Switching signal modification by stage-gain suppression

The first method to provide multiple no-load voltages utilizes the fact that each converter stage nominally doubles the voltage. With zero duty ratio, the converter stage becomes idle and does not change the voltage, i. e., its gain becomes 1. Therefore, if to operate the converter with one idle stage, the total gain will be halved compared to the basic converter. If two stages are idle the gain will be reduced to quarter.

In general, the *n*-stage CMSCC can add up to $(n-1)$ new values of no-load voltages in such a way that the j^{th} no-load voltage is given by:

$$V_{o,oc,j} = V_i \times 2^{n-j}, \ldots j = 0,1,2,..n-1, \qquad (4)$$

where j represents the number of idle stages.

To achieve maximum efficiency, $V_{o,o.c.}$ has to be as low as possible as indicated in (1). For a given reference output voltage V_o^*, the number of idle stages (j) is determined to meet the following condition:

$$V_{o,j+1} < V_o^* < V_{o,j}. \qquad (5)$$

Applying (5) over the entire operation range of the three-stage CMSCC results the nominal efficiency/output voltage characteristics shown in Fig. 2.

By suppressing the gain of one stage, the efficiency is enhanced for the output voltage ranges between 25 % – to –50 % of the maximum value. For a lower voltage, two stages must be idled. For an output voltage near 50 % the efficiency drops to 50 % of its maximum value as the converter operates with $V_{o,oc}=2^n V_i$.

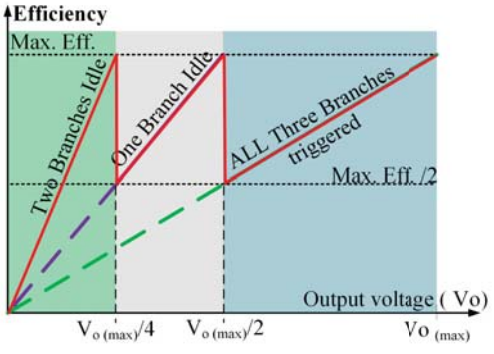

Fig. 2. Nominal efficiency against Vo with 3 No-load voltage

4. 5. Converter circuit modification

The CMSCC circuit has been modified in this paper to allow the capacitor of $C_{2,A}$ or $C_{3,A}$ to be charged directly by V_i, while the other capacitor in the same stage, $C_{2,B}$ or $C_{3,B}$ is charged from the previous stage output. Fig. 3 shows the resultant modified compact modular converter (MCMC). The two switches marked by $Q_{2,E}$ and $Q_{3,E}$ have been added to the original CMSCC design. The charging path indicated by the dashed line allows charging $C_{2,A}$ to V_i. This capacitor can be also charged to the voltage ($V_{C1,A}$+$V_{C1,B}$) as indicated by the solid line.

This provides additional three no-load voltages as follows:

– 3*Vi*: when charging $C_{2,A}$ to *Vi* and $C_{2,B}$ to 2*Vi* by setting the gain of stage 1 to 2 and the gain of stage 3 to 1(idle);

– 5*Vi*: when charging $C_{3,A}$ to *Vi* and $C_{3,B}$ to 4*Vi* by setting the gains of stage 1 and stage 2 to 2;

– 6*Vi:* when charging $C_{2,A}$ to *Vi* and $C_{2,B}$ to 2*Vi* by setting the gains of stage 1 and stage 3 to 2.

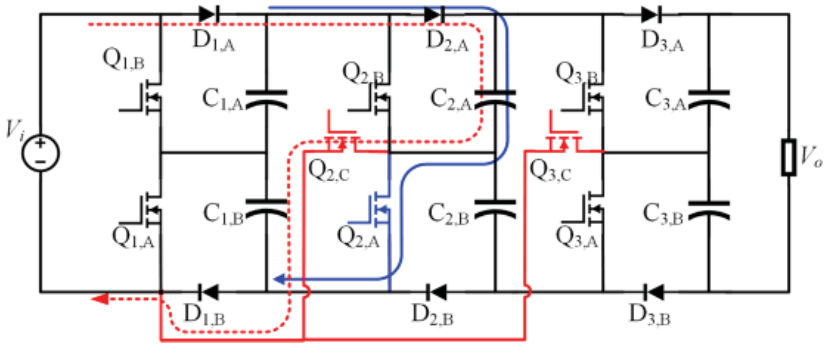

Fig. 3. Modified compact modular converter with two added switches

Table 1 lists the switching patterns for all available no-load voltages. In this table, the switching functions (ϕ_1–ϕ_6) are indicated in Fig. 1, *c*. When the switching signal is zero the corresponding switch is OFF. If a branch is in idle state (the two switching functions are 0's) the sum of corresponding branch capacitors voltages is similar to the preceding stage output voltage and the stage gain is 1. Notice that some levels can be obtained with multiple patterns. The converter output voltage (V_o) is determined as follows:

$$V_o = V_{C3,A} + V_{C3,B}. \qquad (6)$$

With six open circuit voltage levels (2, 3, 4, 5, 6, and 8)**Vi*, the variation of the nominal efficiency over the entire output voltage range is shown in Fig. 4.

Table 1

The switching signals of the MCMC

Stage 1 $Q_{1,A}$, $Q_{1,B}$	Stage 2 $Q_{2,A}$, $Q_{2,B}$, $Q_{2,E}$	Stage 3 $Q_{3,A}$,$Q_{3,B}$, $Q_{3,E}$	$V_o(O.C)$
ϕ_1, ϕ_4	ϕ_3, ϕ_6, 0	ϕ_5, ϕ_2, 0	8Vi
ϕ_1, ϕ_4	ϕ_3, 0, ϕ_6	ϕ_5, ϕ_2, 0	6Vi
ϕ_1, ϕ_4	ϕ_3, ϕ_6, 0	ϕ_5, 0, ϕ_2	5Vi
0 ,0	ϕ_3, ϕ_6, 0	ϕ_5, ϕ_2, 0	4Vi
ϕ_1, ϕ_4	0 ,0, 0	ϕ_5, ϕ_2, 0	4Vi
ϕ_1, ϕ_4	ϕ_3, ϕ_6, 0	0, 0, 0	4Vi
ϕ_1, ϕ_4	0, 0 ,0	ϕ_5, 0, ϕ_2	3Vi
0, 0	ϕ_3, ϕ_6, 0	ϕ_5, 0, ϕ_2	3Vi
ϕ_1, ϕ_4	0, 0, 0	0, 0, 0	2Vi
0, 0	ϕ_3, ϕ_6, 0	0, 0, 0	2Vi
0, 0	0, 0, 0	ϕ_5, ϕ_2, 0	2Vi

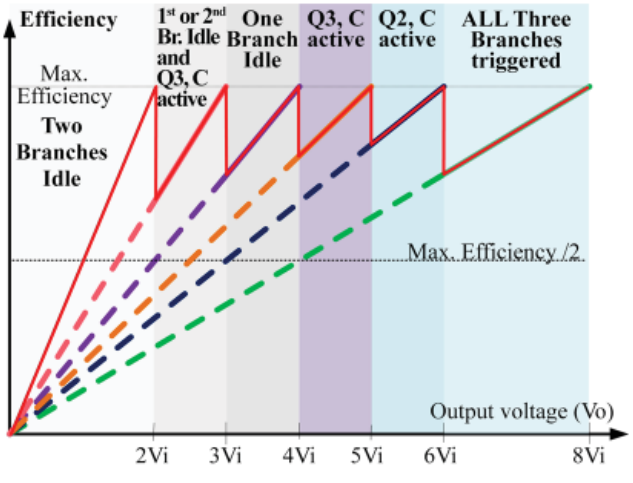

Fig. 4. Nominal efficiency against the output voltage with 6 no-load voltages of the modified compact modular converter

To achieve an adjustable output voltage in the range (V_m<V_o≤V_n); where V_m and V_n are two consecutive open circuit voltages; the control signals generated as follows.

For stages 1 and 3, the switching signals as described in Table 1, i. e., with a 50 % (or 0) duty ratio.

For stage 2, the switching signals indicated in Table 1 are subjected to duty ratio adjustment via a PI-voltage controller.

4. 6. Simulation models of the modified converter and controls.

To examine the performance of the proposed MCMC, the Simulink model shown in Fig. 5 has been constructed. The model parameters are given in Table 2.

Table 2

Simulated converter model parameters

Element	Part No.	Parameters
Source	537-7305 lead acid battery	12 V, 14 mΩ
Load	–	100 Ω resistor
MOSFET	FDD86250-F085	Ron=22 mΩ, Body diode: VF=0.78 V, Rs=4 mΩ
Diode	VS-30CPQ15 (Vishay)	VF=450mV, ROFF (snubber)=500 kΩ
Capacitor	EZPV600 100 LT	100 μF, ESR=5.1 mΩ

To model output voltage regulation by duty cycle adjustment, the feedback control loop shown in Fig. 6 has been developed. The PI-controller has a proportional and integral gains of 0.1 and 10 respectively. Shifted carrier signals have been used to generate the shifted switching signals (ϕ_1–ϕ_6). The PI-controller output has been compared to the 1/6-cycle-shifted sawtooth waves to impose the duty ratio to the six switching signals.

To implement the controller of the MCMC with multiple no-load voltages based on Table 1, an outer open circuit voltage and inner duty cycle adjustment control loops have been designed as shown in Fig. 7. In this model, the nominal gain is determined as follows:

$$G_{nom} = \left\lceil \frac{V_o^*}{V_i} \right\rceil, \tag{7}$$

where $\lceil x \rceil$ stands for rounding up of x.

The hysteresis controller is added to correct the initial value of G_{nom} calculated according to (7). When the inner loop saturated, the hysteresis controller increases G_{nom} to the next value if the output voltage is still below the reference. The inner loop is similar to the PI controller used to reduce the voltage by controlling the duty ratio of the basic CMSCC shown in Fig. 6.

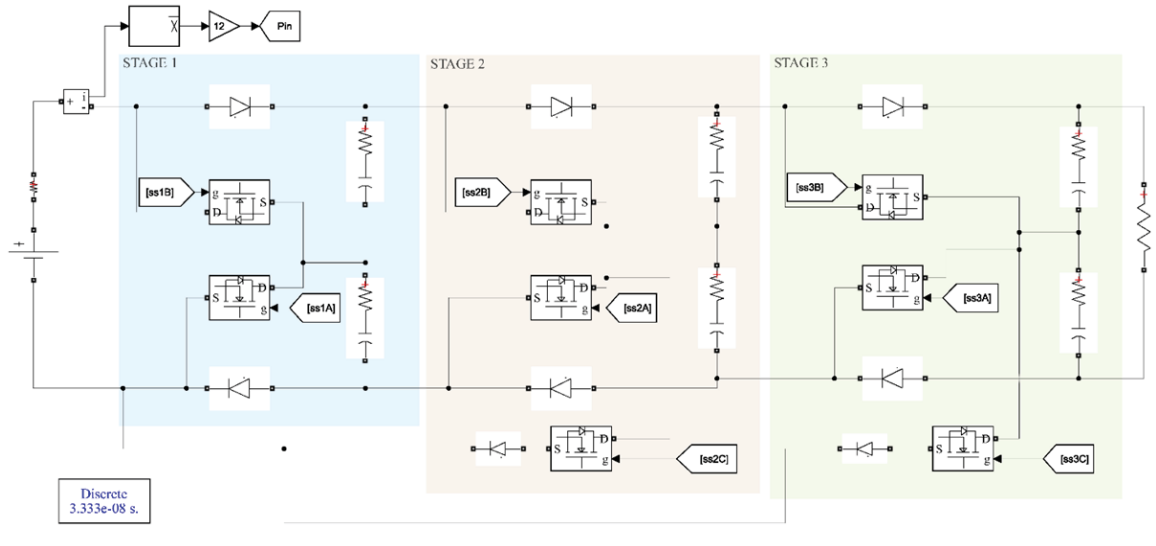

Fig. 5. Simulink model of the converter system

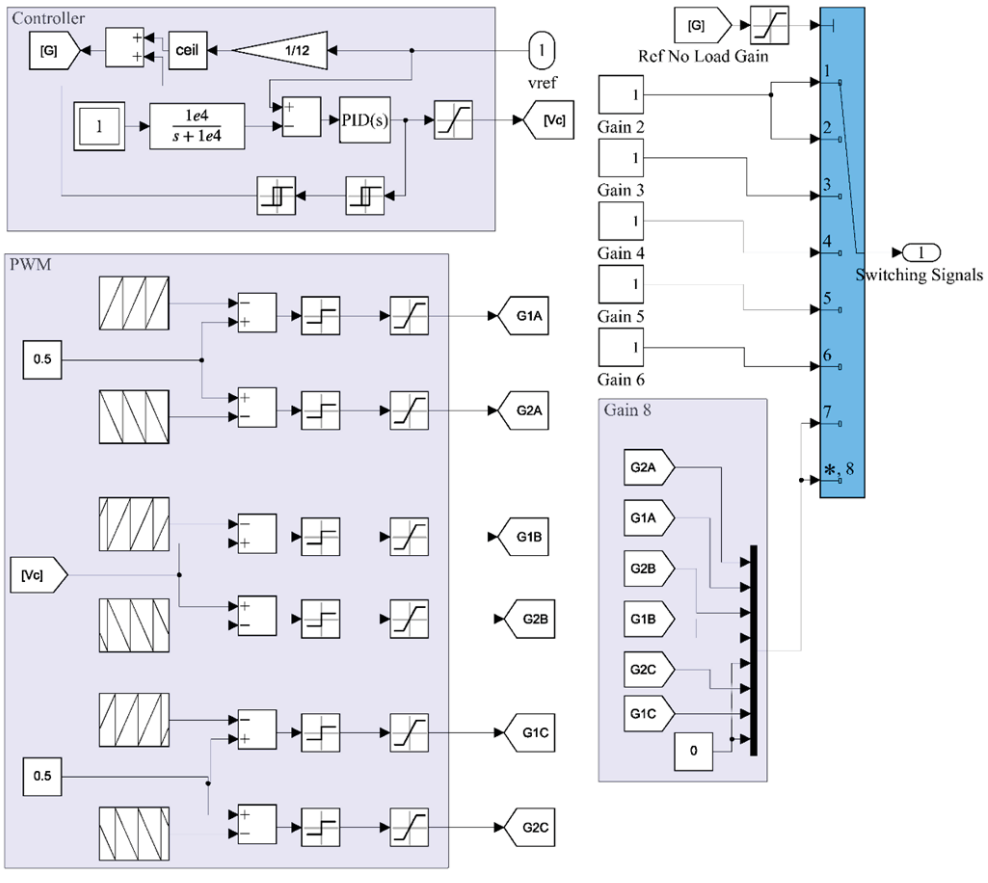

Fig. 6. Duty ratio regulator for shifted switching signals

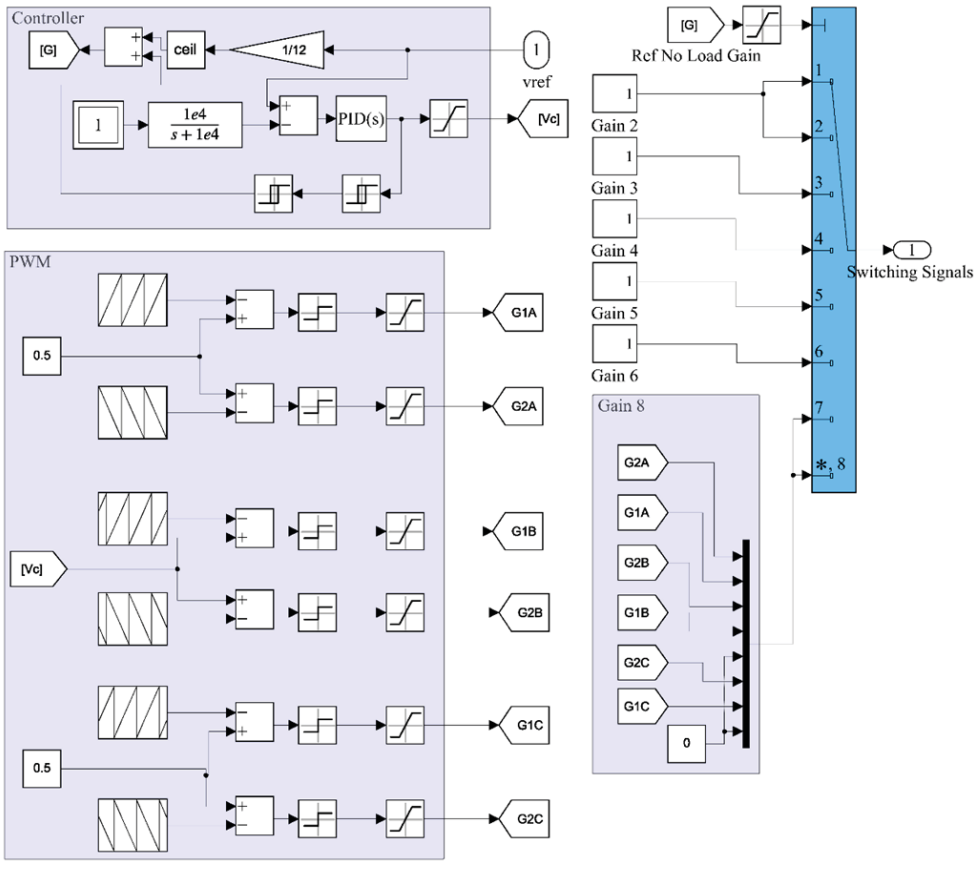

Fig. 7. Voltage controller model to produce 6 no load voltages of the modified compact modular converter

5. Results of performance of the modified compact modular converter

5. 1. Duty cycle adjustment

To set a switching frequency near SSL, the output voltage variation with the frequency has been examined first. The variation of the load voltage against the switching frequency for common mode and shifted switching are shown in Fig. 8.

The output resistance has been calculated at different frequencies by comparing the no-load output voltage ($V_{O,OC}$) and the load voltage ($V_O(f_{sw})$) and the results are shown in Fig. 9. The converter output resistance is calculated as follows:

$$R_o(f_{sw}) = \frac{V_{o,o.c} - V_o(f_{sw})}{\frac{V_o(f_{sw})}{R_L}}. \quad (8)$$

At low switching frequencies, the shifted switching signals described in Fig. 2, *c*, provide considerable increase in output voltage compared to the common mode signals shown in Fig. 2, *b*. Fig. 9 reveals that the converter output resistance is reduced by more than 30 % at switching frequencies below 1kHz while the switching signals shifting has no visible effect as the switching frequency exceeds the SSL of about 20 kHz. Accordingly, the switching frequency has been set to 20kHz which is the frequency of the carrier signals in Fig. 6 and Fig. 7.

To apply the voltage of the CMSCC, the reference voltage which changes from 20 to 90 V in 10 V steps is considered. Fig. 10 shows the variation of the output voltage and efficiency. This figure shows that the converter effectively tracks the reference output voltage. The efficiency characteristics resembles (1); i. e., proportional to the output voltage.

At low voltage range, the efficiency drop is very significant and unacceptable. The maximum output voltage when the controller saturates is about 87.8 V which is less that the maximum reference value of 90 V.

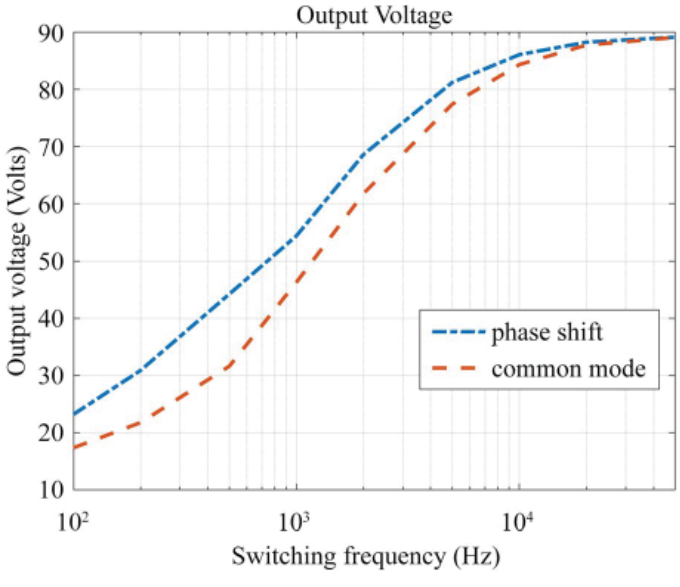

Fig. 8. The effect of changing the switching frequency on the output voltage

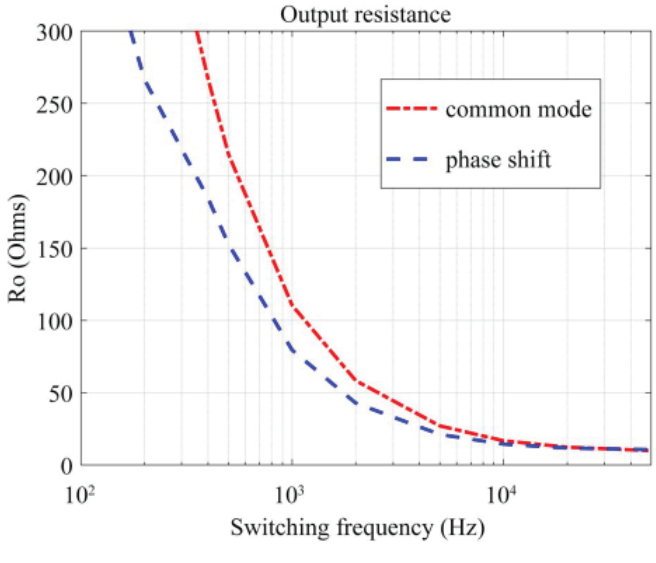

Fig. 9. Converter output resistance variation with the switching frequency

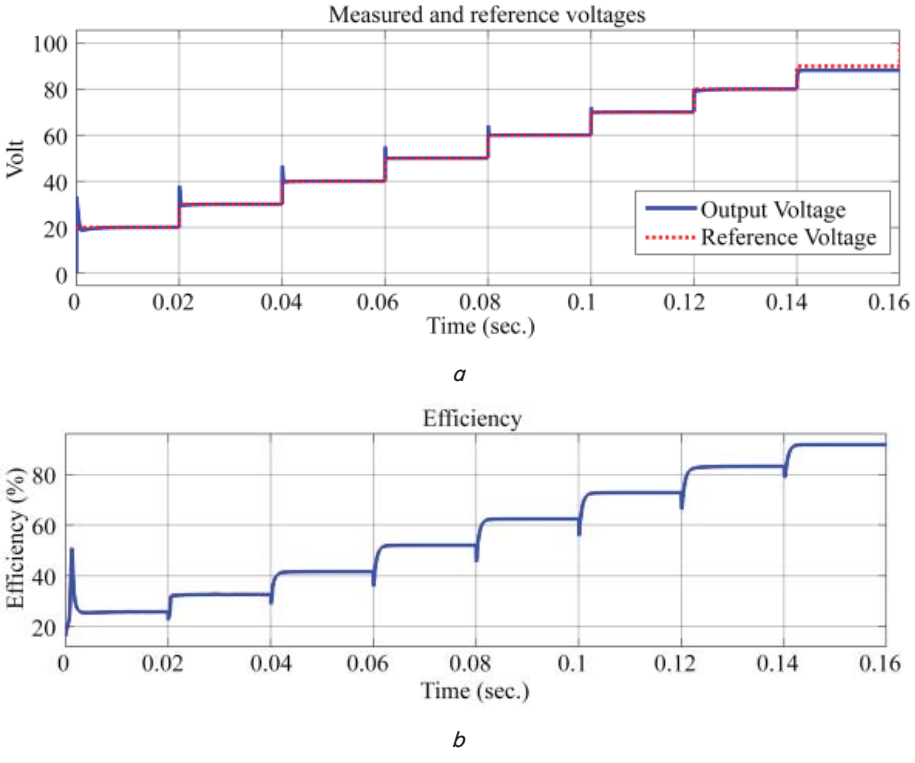

Fig. 10. Controlling the output voltage by adjusting the duty ratio: *a* – stepped reference voltage and the output voltage; *b* – the efficiency with shifted switching signals

5. 2. Efficiency enhancement

The converter operation has been simulated after disabling 0, 1 or 2 stages to provide three values of no load gain: 8, 4 and 2. The PI controller regulates the duty ratio of the switches of stage (2) only to reduce the ripple. For a stepped reference voltage, the variation of the output voltage and the efficiency are shown in Fig. 11. The minimum efficiency obtained for the stepped reference is about 58 % of the maximum efficiency.

The stage suppression is not applicable when the output voltage is required to be more than 50 % of its maximum value and therefore no efficiency improvement is obtained in this range.

The MCMC operation has been simulated with stepped reference output voltage. The reference and resultant output voltages and the corresponding converter efficiency are shown in Fig. 12. It can be seen that the minimum efficiency is about 80 % of the maximum value (when V_o is unregulated).

The simulation result of efficiency at different output voltages are compared to the expected performance for the various operations modes as shown in Fig. 13. This figure reflects the agreement between simulated and theoretical efficiency and also shows the effect of switching modification especially in the low range of output voltage.

The converter efficiency for various values of output voltages and the three operation modes are given in Table 3. The average efficiency is calculated as the mean efficiency for the eight output voltages.

Table 3

Simulated efficiency (%) of the UMSCC with and without stage gain suppression and the modified converter

Reference Voltage (V)	Shifted Switching (one no-load voltage) efficiency (%)	Stage Suppression (3 no-load voltages) efficiency (%)	Modified (with duty ratio and G control) efficiency (%)
20	21.7	83.3	83.3
30	30.5	62.52	83.2
40	41.6	83.3	83.3
50	52.08	52.08	83.4
60	62.4	62.48	83
70	72.9	72.9	72.6
80	83.3	83.3	83.4
90 V_{out}=87.77(max)	91.2	91.2	91.2
Averages efficiency	57.71	73.91	82.9

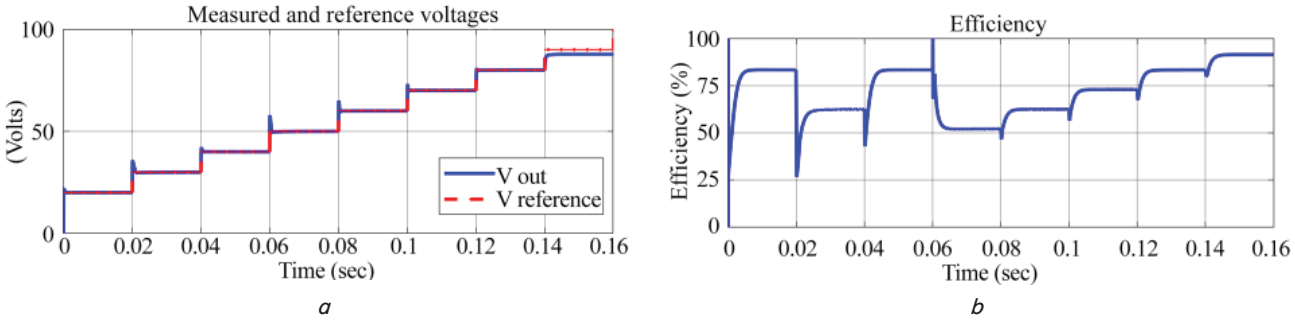

Fig. 11. Efficiency enhancement by stage suppression: *a* – reference voltage and output voltage; *b* – efficiency

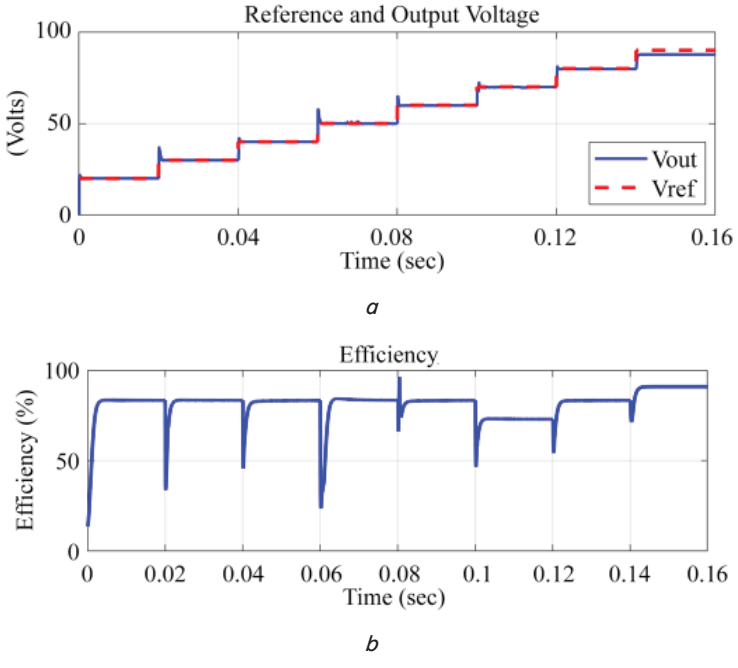

Fig. 12. Performance of the MCMC with six no load voltage levels and closed loop algorithm selection: *a* – reference voltage and output voltage; *b* – efficiency

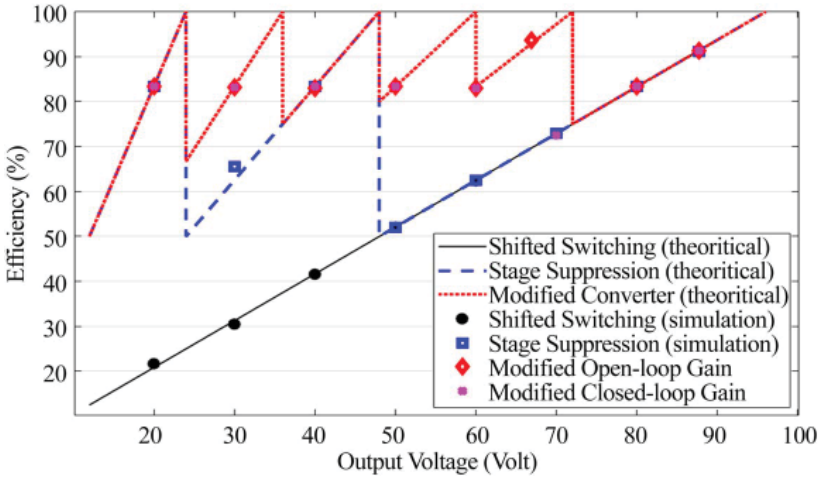

Fig. 13. Efficiency versus output voltage using three control approaches

Table 4 presents a comparison between the suggested MCMC and other designs reported in the literature.

Table 4

Comparison between the proposed converter and other SCC converters with multiple no-load voltages

Parameter	MCMC	Ref [18]	Ref [19]	Ref [16]
No. of switches	8	12	17	14
Number of capacitors	6	8	8	4
No. of voltage steps	6	4	5	21
Maximum gain	8	8	9	8
Total switches voltage rating	5*Vo*	6*Vo*	5*Vo*	8*Vo*
Total capacitor voltage rating	1.75*Vo*	4*Vo*	1.8*Vo*	1.875*Vo*
Modular design	Y	N	N	N
Bidirectional power flow	N	N	Y	N
2-phase cycle	Y	Y	Y	N

6. Discussion of the voltage regulation and efficiency results

The objective of this work is twofold, on the one side Voltage regulation by duty cycle adjustment. This task has been achieved in CMSCC by regulating the duty ratio of the switching signal as shown in Fig. 10, *a*. The results show that output voltage follows the reference almost identically for any reference voltage from 20 V up to the maximum output voltage, which is about 87.8 V. For reference voltages beyond this level the controller saturates and the output voltage remains constant. Voltage regulation by duty ratio control is applied by the inner voltage control loop on the proposed MCMC, Fig. 11, *a*, 12, *a* show that the with duty cycle regulation it is always possible to obtain a reference voltage below the maximum unregulated value.

Voltage regulation by switching pulse duty ratio leads to poor efficiency as shown in Fig. 10, *b*. On the other hand, to improve the efficiency by the stage suppression and modified design (MCMC) suggested in this paper. By idling one or two of the converter cascaded modules (stages), the converter efficiency has been enhanced as seen by comparing Fig. 11, *b* to Fig. 10, *b*. Stage suppression, however, does not treat the low efficiency defect for the gain in the region near and above 50 % of the maximum gain. The introduction of new output no-load voltages (3*Vi*, 5*Vi* and 6*Vi*) through the bypass switches Q2,C and Q3,C has a considerable effect on the converter efficiency as shown in Fig. 12, *b*. Fig. 13 shows the efficiency improvement of the CMCM compared to the state suppression and duty control of the basic CMSCC for output voltage values of 30, 50 and 60 V corresponding to

the nominal gain values of 3, 5 and 6 respectively introduced in this design. It is seen form Table 3 that the modified converter effectively treats the low efficiency problem of the CMSCC. The minimum efficiency of the modified converter is close to 80 % of the maximum efficiency of the basic CMSCC and the average efficiency over the entire voltage control range is about 90 % of the maximum efficiency of the basic converter.

Table 4 lists some features of the CMCM and other variable voltage SCC presented in the literature. Compared to other SCCs of two-phase cycle suggested in [18, 19]; the MCMC has the maximum number of no-load voltages, minimum number of switches and total switch voltage rating. It has also the minimum total capacitor voltage ratings. The multiphase cycle converter [16], however, provides the maximum number of voltage steps at the expense of large number of series switches in the current path.

Efficient voltage regulation of CMSCC is the aim of this study. The aim has been achieved by two tasks, the first is to impose voltage regulation done by one or two voltage control loops and the results are shown in Fig. 10, *a*, 11, *a*, 12, *a*. The second task, the efficiency improvement is realized by the presented MCMC design and results presented in Fig. 13 and Table 3 demonstrate the achieved improvement.

From Fig. 13, it can be seen that that with modified converter and 70 V output voltage the converter does not follow the nominal efficiency characteristics drawn in broken line. Due to the voltage drop across Ro, the 70 V reference voltage cannot be achieved when the nominal gain is 6. The hysteresis gain controller actives next gain value (8) and the converter operated with open circuit voltage of 96 V. The large difference between the output and open circuit voltage causes the efficiency drop in this case. With open loop nominal gain control, the gain is set to 6 and efficiency follows the nominal efficiency line as shown in Fig. 13. In open loop mode, however, the output voltage dose not ensure realization of reference values.

Despite its abovementioned advantages, the MCMC converter inherited the problem of relatively large output resistance of the CMSCC, this forms the main limitation specially for high power applications.

A further work may consider implementing the proposed converter topology using recent state of art switching devices such as SiC and GaN.

7. Conclusions

1. The SCC gain has been controlled precisely by tunning the duty ratio of the switching signals. A voltage negative feedback loop and a PI controller is used to realize this objective. The designed converter controller applies an outer no-load voltage controller besides a PI-inner loop voltage regulator. The inner loop adjusts the switching signal duty ratio to track the reference voltage. The outer loop applies a hysteresis controller to increase the no-load voltage if the voltage drop across Ro plus the reference voltage is higher that the nominal no load voltage next higher to reference voltage.

2. When the duty ratio is controlled to produce an adjustable output voltage, the efficiency of the basic CMSCC drops considerably. To solve this problem, six no-load voltages have been provided by two measures: altering the switching method and modifying the converter circuit. The switching signals has been modified to change the no-load voltage while maintaining a two-phase cycle for all operation modes. The proposed converter circuit modifications add only two (n–1) switching devices to the three (n) stage converter; and maintains the modular design of the original CMSCC at least to some extent. On-load the efficiency of the unregulated switched capacitor converter is found to be 91.2 %. when the output voltage is regulated down to 23 % of the no load voltage, the average of the efficiency has been improved from 57 % for the basic CMSCC to 83 % for the proposed CMCM.

Conflict of interest

The authors declare that they have no conflict of interest in relation to this research, whether financial, personal, authorship or otherwise, that could affect the research and its results presented in this paper.

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Data availability

Data will be made available on reasonable request.

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