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This study examines CMOS ring oscillators that are used as converters of capacitive sensor parameters. The issue with most analytical models is their assumption of symmetric stage loading, making them inaccurate for the topology where a sensor connection to a single node introduces asymmetry. The lack of a validated model for 45-nm technology complicates the design of sensitivity and energy efficiency.

An analytical model for the capacity to frequency converter that accounts for asymmetric loading has been built and verified. The model is based on the physical principle of summing asymmetric stage delays and a linear approximation of inverter delay versus load capacitance.

A parametric analysis was performed in LTspice (sensor capacitance C_{sensor} is from 0 to 2.5 pF) to verify the model. It was determined that the oscillation period has a quasi-linear dependence on capacitance; therefore, the frequency dependence is hyperbolic. The proposed model predicts the frequency with a maximum relative error of no more than 1.55% over the entire simulation range (21.17–29.96 MHz) compared to SPICE data.

Key metrics have been analyzed: the average sensitivity is 3.52 MHz/pF, while the instantaneous sensitivity is non-linear, decreasing from 5.57 MHz/pF to 2.15 MHz/pF. Power consumption increases slightly (151.3–155.7 μW), as the capacitance growth is compensated by the frequency drop. Energy per cycle (E_{cycle}), conversely, increases almost linearly (5.05–7.35 pJ) with a slope of 0.92 pJ/pF. This closely matches the theoretical value of VDD^2 = 1.0 pJ/pF, confirming the dominance of dynamic power consumption.

The proposed model allows engineers to accurately predict and design the capacity-to-frequency characteristics, sensitivity, as well as power consumption of compact integrated sensor interfaces

Keywords: ring oscillator, complementary metal-oxide-semiconductor structure, micro-electro-mechanical systems, frequency, capacitive sensor

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DESIGN OF A RING OSCILLATOR FOR DIRECT CONVERSION OF CAPACITANCE INTO FREQUENCY IN CAPACITIVE SENSOR INTERFACES

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1. Introduction

The rapid development of the Internet of Things (IoT), wearable devices, and wireless sensor networks is leading to more complex requirements for integrated circuits [1]. The key elements of such systems are microelectromechanical systems (MEMS), which convert physical quantities into electrical signals [2]. Capacitive MEMS sensors, such as accelerometers, gyroscopes, pressure, and humidity sensors, are particularly common. They have gained popularity due to their high sensitivity and low power consumption [3].

The effectiveness of such a sensor system largely depends on the readout circuit that converts small changes in capacitance (from femtofarads to picofarads) into a digital signal. There are a number of problems in conventional techniques for implementing such interfaces. One such approach is the conversion of capacitance into voltage, which requires analog-to-digital conversion (ADC) stages and increases the total area on the chip and power consumption [4]. There is also a more sophisticated approach, such as the sigma-delta modulator [3], which provides high resolution but is too complex for many applications and can dissipate significant power [5].

There is a need to investigate alternative MEMS sensor readout schemes that are simple, compact, and energy efficient. One such alternative approach is direct capacitance-to-frequency conversion [6]. This approach uses a capacitive sensor as an element that affects the frequency of the oscillator. Changing the capacitance of the sensor directly modulates the output frequency of the oscillator. This frequency signal is quasi-digital and can be easily digitized using a simple counter integrated into a microcontroller [7].

Among the different types of generators, ring oscillators are well-known candidates for capacitance-to-frequency conversion due to the following advantages:

– compactness: ring oscillators are built exclusively on the basis of an odd number of inverters and do not require the use of passive components. In particular, it is shown in [8] that the absence of inductors allows for a significant reduction in the area on the chip. Study [9] also confirms that small

size is a critical advantage in the implementation of systems on a chip for autonomous devices;

– high level of integration: they are fully implemented in a standard CMOS process, which makes it possible to easily integrate them on the same chip with a sensor and digital logic;

– scalability: their characteristics are easily scaled with the transition to more modern technological nodes.

In practice, designing on submicron technologies, such as 45-nm CMOS [10], can achieve high performance and a high degree of integration. This in turn will make it possible to reduce the cost, size, and power consumption of the end device. But the behavior of transistors on such nodes is complex, nonlinear, and significantly depends on parasitic effects and process variations [11]. In particular, studies of the design and technological features of the formation of semiconductor structures indicate a significant impact of technological dispersion on the output characteristics of active elements [12]. For the effective design of capacitance-to-frequency conversion interfaces based on ring oscillators, analytical models are needed that relate the sensor capacitance to the output frequency and power consumption.

Therefore, studies aimed to model, analyze, and characterize ring oscillator models for capacitance-to-frequency conversion on 45-nm CMOS technology are relevant for building a methodological basis for designing energy-efficient and compact MEMS sensor reading circuits.

2. Literature review and problem statement

There is a fundamental dilemma in designing analog interfaces, such as capacitance-to-frequency converters, on modern deep submicron CMOS technologies (e.g., 45 nm). On the one hand, scaling technology degrades key analog parameters, such as intrinsic transistor gain and increases variability [13]. On the other hand, it improves the speed and density of digital elements [13]. In particular, improvements in hardware arithmetic algorithms minimize resource consumption and increase system performance [14]. This stimulates the global trend towards "digitized" analog circuits, where analog functions are increasingly implemented using digital standard elements [13].

However, a detailed analysis of related literature reveals that a number of problems remain unsolved. Despite the development of "digitized" analog circuits, their performance in many cases still does not reach the level of the best conventional analog solutions [13]. In addition, matrix multiplier structures are characterized by low hardware utilization, and tree-like algorithms (such as Wallace or Dadd schemes) have an irregular structure, which complicates their hardware implementation [14]. The main reason for this is the limited supply voltage margin and the difficult trade-off between speed, accuracy, and power consumption [13].

Modern research on the conversion of physical quantities into frequency based on oscillators offers various approaches to resolving these contradictions. In [1], a 22-nm FDSOI oscillator adapted for a voltage of 0.4 V is presented. The scheme provides a frequency of 666.8 MHz with a power consumption of 10.23 μW and has a linear sensitivity of 2.63 MHz/nA. However, despite the high speed and energy efficiency, such solutions often have a limited dynamic range of input currents, which requires additional optimization for sensor applications. Study [15] describes the use of dynamic leakage suppression logic, which makes it possible to achieve consumption of 1.4–1.6 pW at a voltage of 0.3 V. However, due to the operation of transistors under the subthreshold mode, the speed of such devices is limited to operation in the low-frequency (Hz) spectrum, which makes them unsuitable for high-speed measurement systems.

An option to overcome these limitations is the capacitance-to-digital converter. In such architectures, the capacitance becomes a time interval that is digitized by a time-to-digital converter [16]. For example, the iterative discharge method provides high resolution [6]. However, these solutions are much more complex than a simple generator, which increases the crystal area.

It is the direct conversion approach that is used in [8] on 45-mm technology. The operation of the circuit is shown in a wide capacitance range (1–100 pF). However, the results are limited only by simulation. In [17], an ultra-high sensitivity of 180 aF was achieved. However, this result was obtained in a very narrow range (± 0.5 pF), which limits the practical application of the method.

The cause of the design problems is the inaccuracy of the basic models. Most works rely on formula $f_{osc} = 1 / (2N \cdot t_d)$ for a symmetrical load [1]. But connecting the sensor to one node creates asymmetry. N–1 cascades have a load C_{load}, and the sensor node $C_{load} + C_{sensor}$. Under such conditions, the symmetric model becomes inaccurate.

In [13], the effect of asymmetry is investigated using the example of ring amplifiers. It is shown that symmetry breaking requires the implementation of complex stabilization techniques, such as "dead zones". But this proves that the asymmetric ring becomes a complex dynamical system. It is no longer described by simplified, generally accepted basic models.

According to [18], when moving to 45 nm technology, physical limitations become critical for the accuracy of calculations. In [19], it was confirmed that the delay in such structures obeys a nonlinear alpha-power law. Asymmetric loading additionally distorts the waveform across the ring [20]. This creates a nonlinear system that is difficult to calculate manually without using a specialized model.

Thus, a critical analysis revealed a contradiction between the need to design compact energy-efficient interfaces of direct capacitance-frequency conversion and the inaccuracy of existing mathematical apparatus for their calculation. A current problem is the lack of a refined analytical model of the ring oscillator, which would simultaneously take into account the nonlinear physics of the 45 nm technological process and the asymmetry of the node load caused by the sensor connection. This limits the ability to engineer predictions of transducer sensitivity and linearity, forcing designers to rely on lengthy and iterative SPICE simulations.

3. The aim and objectives of the study

The aim of our study is to establish an analytical dependence of the oscillation frequency of a five-stage ring oscillator (45-nm CMOS) on the magnitude of the asymmetric capacitive load of the node to improve the accuracy of the capacitance-frequency conversion. This could provide an opportunity to devise a basic design methodology for engineers, which would allow them to quickly evaluate and optimize the key parameters of simple capacitance-to-frequency converters for their further integration into energy-efficient MEMS interfaces. This basic methodology will be practically useful for design engineers to predict and optimize the characteristics of capacitance-to-frequency conversion, sensitivity, linearity, and energy efficiency of integrated interfaces for capacitive MEMS sensors.

To achieve the goal, the following tasks were set:

– to build a general analytical model of the dependence of the period (and frequency) of oscillations on the sensor capacitance, based on the physical principle of summation of delays of asymmetric cascades, and to approximate this dependence to an empirical formula suitable for engineering calculations;

– to conduct parametric modeling in LTspice, changing the sensor capacitance (C_{sensor}) in the range of 0–2.5 pF, to analyze the key operating characteristics of the resulting capacitance-to-frequency converter: period and frequency sensitivity and their dependence on C_{sensor}, conversion linearity, power consumption (P) and energy per cycle (E_{cycle});

– to verify the proposed analytical model by comparing the calculated data with the simulation results;

– to evaluate the energy characteristics of the model – power consumption (P) and energy per cycle (E_{cycle}).

4. Materials and methods

The object of our study is ring CMOS oscillators as transducers of capacitive sensor parameters.

The principal hypothesis assumes that the total oscillation period T_{osc} can be approximated with high accuracy (< 2%) as a linear function of the added sensor capacitance C_{sensor}, i.e., $T_{osc}(C_{sensor}) \approx T_0 + S_T \cdot C_{sensor}$. This hypothesis is based on the fact that the total period is determined by the sum of the delays of all stages $T_{osc} = 2 \cdot \sum \tau_{pi}$ [21], and the delay of an individual stage τ_p in the first approximation linearly depends on its load capacitance C_{load} [18]. It is expected that the dependence of the frequency on the capacitance will be nonlinear (hyperbolic).

To simplify the study, simulations are carried out in the LTspice environment using the nominal parameters of the 45-nm High Performance CMOS model [22] at a temperature of 27°C. Variations in the technological process, voltage, and temperature are not taken into account. The intrinsic parasitic capacitances of the transistors are considered an integral part of the inverter and at the same time a significant external load C_{load} = 1 pF is added to each node. This load dominates the parasitic capacitance, stabilizing the base frequency of the generator, but at the same time increasing its power consumption.

The MEMS sensor is modeled as an ideal variable capacitor C_{sensor} without parasitic resistances or inductances.

The research was carried out using simulation and analytical modeling methods.

The ring oscillator circuit was implemented in LTspice and is shown in Fig. 1.

The circuit consists of five identical CMOS inverters connected in a ring. The supply voltage (*VDD*) is 1.0 V. The circuit is asymmetric: the first four nodes have a capacitive load C_{load} = 1 pF each (capacitors C1, C2, C3, C4). The fifth node, which is the output of the last inverter and the input of the first, has a capacitive load $C_{load} + C_{sensor}$ (capacitors C5 and C6).

The ring oscillator circuit in LTspice uses CMOS models of 45 nm transistors [22]. The width of the PMOS transistors is W_p = 400 nm, the width of the NMOS transistors is W_n = 160 nm. The width ratio is W_p / W_n = 2.5, which is typical for optimization under symmetrical signal edges. The length of both types of transistors is L = 45 nm.

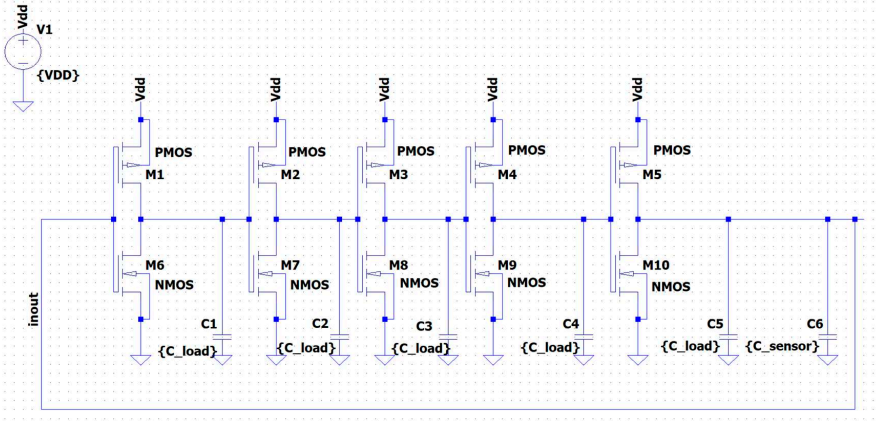

Fig. 1. Ring oscillator diagram

The analysis was performed using the .tran (transient analysis) directive using the parametric analysis .step param C_sensor 0p 2.5p 0.25p. This command performs 11 simulations, sequentially increasing the sensor capacitance from 0 pF to 2.5 pF in 0.25 pF steps.

The built-in .meas directives were used to collect data:

– .meas TRAN T: measurement of the period T of the signal V(inout);

– .meas tran F param 1 / T: calculation of the frequency F;

– .meas tran Idd AVG I(V1): measurement of the average current consumption I_{dd};

– .meas tran P param-VDD * Idd: calculation of the average power P;

– .meas tran Ecyc param P / F: calculation of the energy consumed per cycle.

The symmetrical operation mode of the ring oscillator, which serves as a reference point, is achieved provided that the sensor capacitance is 0 pF. In this case, each of the 5 stages of the generator has the same capacitive load of 1 pF.

According to the simulation results, the following basic parameters are fixed for this symmetrical case:

– period T_0 = 33.38 ns (3.33767 10-8 s);

– frequency F_0 = 29.96 MHz (2.9961·107 Hz);

– average current $I_{DD,0}$ = 151.31 μA (0.000151312 A);

– average power P_0 = 151.31 μW (0.000151312 W, since VDD = 1.0 V);

– energy per cycle $E_{cycle,0}$ = 5.05 pJ (5.0503·10-12 J);

– duty cycle was 51.13%.

The analytical model is based on the propagation delay equations of the CMOS inverter. The oscillation frequency of the N-stage ring oscillator is determined by the total period, which is equal to twice the total propagation delay of all stages [23].

5. Results of research on the conversion of sensor capacitance into frequency of a five-stage ring oscillator using 45 nanometer technology

5. 1. Analytical model of the oscillation period of an asymmetric ring oscillator

When $C_{sensor} > 0$, the symmetry of the ring oscillator is broken. The load at the *inout* node (Fig. 1) becomes $C_{load} + C_{sensor}$, while at the other (N – 1) nodes it remains C_{load}.

The total oscillation period T_{osc} for an asymmetric ring oscillator with odd N is defined as the doubled sum of the delays of all stages

$$T_{osc} = 2 \cdot \sum_{i=1}^{N} \tau_{pi} = 2 \cdot \left(\left(N - 1 \right) \cdot \tau_{p\_base} + \tau_{p\_asym} \right), \quad (1)$$

where τ_{p_base} is the delay of the symmetrical cascade (with load C_{load}), and τ_{p_asym} is the delay of the asymmetrical cascade (with load $C_{load} + C_{sensor}$).

The delay of the CMOS inverter, according to the first-order RC model, can be approximated as a linear function of the load capacitance C_{load}

$$\tau_p \left(C_{load} \right) \approx \tau_{int} + K \cdot C_{load}, \quad (2)$$

where τ_{int} is the internal delay of the inverter (at $C_{load} = 0$), and K is a coefficient that depends on the transistor parameters (width to length ratio W/L) and the supply voltage VDD.

By substituting expression (2) into equation (1):

$$\tau_{p\_base} = \tau_{int} + K \cdot C_{load};$$

$$\tau_{p\_asym} = \tau_{int} + K \cdot \left(C_{load} + C_{sensor} \right);$$

$$T_{osc} = 2 \cdot \left(\left(N - 1 \right) \cdot \tau_{p\_base} + \left(\tau_{int} + K \cdot C_{load} + K \cdot C_{sensor} \right) \right);$$

$$T_{osc} = 2 \cdot \left(\left(N - 1 \right) \cdot \tau_{p\_base} + \left(\tau_{int} + K \cdot C_{load} \right) + K \cdot C_{sensor} \right).$$

Since $\tau_{int} + K \cdot C_{load}$ is nothing but τ_{p_base}, then:

$$T_{osc} = 2 \cdot \left(\left(N - 1 \right) \cdot \tau_{p\_base} + \tau_{p\_base} + K \cdot C_{sensor} \right);$$

$$T_{osc} = 2 \cdot \left(N \cdot \tau_{p\_base} + K \cdot C_{sensor} \right);$$

$$T_{osc} = 2 \cdot N \cdot \tau_{p\_base} + 2 \cdot K \cdot C_{sensor}.$$

The expression $2 \cdot N \cdot \tau_{p\_base}$ is the base period of the symmetric generator T_0. Denoting $2 \cdot K \cdot C_{sensor}$ as the new coefficient S_T (period sensitivity), the final model is obtained, confirming the hypothesis

$$T_{osc} \left(C_{sensor} \right) = T_0 + S_T \cdot C_{sensor}. \quad (3)$$

Accordingly, the dependence of the output frequency f_{osc} on capacitance will take the form of an inverse function

$$f_{osc} \left(C_{sensor} \right) = \frac{1}{T_0 + S_T \cdot C_{sensor}}. \quad (4)$$

The obtained expression (4) indicates that the characteristic of the "capacitance-frequency" transformation has a pronounced hyperbolic character.

5. 2. Operating characteristics of the converter according to the results of SPICE simulation

The results of parametric modeling are systematized in Table 1, which gives the characteristics of the converter under two modes: time (capacitance-period) and frequency (capacitance-frequency).

Converter characteristics:

1. Capacitance-period mode.

The dependence of the period on the sensor capacitance is shown in Table 1. The period increment decreases with increasing capacitance: the first 0.25 pF add 1.63 ns, while the last 0.25 pF add only 1.17 ns.

The maximum and minimum local sensitivities are calculated from the following formulas:

$$S_{T,\max} = \frac{\left| T_{step2} - T_{step1} \right|}{C_{step2} - C_{step1}} = \frac{\left| 35.00 - 33.38 \right|}{0.25} = 6.48 \left(\text{ns/pF} \right),$$

$$S_{T,\max} = \frac{\left| T_{step11} - T_{step10} \right|}{C_{step11} - C_{step10}} = \frac{\left| 47.23 - 46.06 \right|}{0.25} = 4.68 \left(\text{ns/pF} \right).$$

The calculation showed that the maximum local sensitivity of the period (at $C_{sensor} \approx 0$ pF) is $S_{T,\max} = 6.48$ ns/pF. Accordingly, the minimum local sensitivity at maximum load ($C_{sensor} \approx 2.5$ pF) was $S_{T,\min} = 4.68$ ns/pF.

The average sensitivity over the entire range is calculated as the slope of the line

$$S_{T,avg} = \frac{\Delta T}{\Delta C} = \frac{T_{\max} - T_{\min}}{C_{\max} - C_{\min}} = \frac{47.23 - 33.38}{2.5 - 0.5} = \frac{13.86}{2.5} = 5.54 \left(\text{ns/pF} \right).$$

The average sensitivity was $S_{T,avg} = 5.54$ ns/pF.

The dynamics of sensitivity changes are visualized in Fig. 2.

Table 1

Results of modeling the time and frequency characteristics

Simulation step	C_{sensor} (pF)	T_{sim} (ns)	F_{sim} (MHz)
1	0.00	33.38	29.96
2	0.25	35.00	28.57
3	0.50	36.56	27.35
4	0.75	38.07	26.27
5	1.00	39.52	25.30
6	1.25	40.92	24.44
7	1.50	42.28	23.65
8	1.75	43.59	22.94
9	2.00	44.85	22.30
10	2.25	46.06	21.70
11	2.5	47.23	21.17

The system is nonlinear; its characteristic can be fitted to a linear model $T_{osc}(C_{sensor}) \approx T_0 + 5.54 \cdot C_{sensor}$ with an error of 1.52%.

2. Capacitance-frequency mode.

The dependence of frequency on capacitance and the plot of S_F sensitivity change are shown in Fig. 3.

The maximum sensitivity is calculated as the ratio of the frequency change to the capacitance change between the first and second steps

$$S_{F,\max} = \frac{\left| F_{step2} - F_{step1} \right|}{C_{step2} - C_{step1}} = \frac{\left| 28.57 - 29.97 \right|}{0.25} = 5.56 \left(\text{MHz/pF} \right).$$

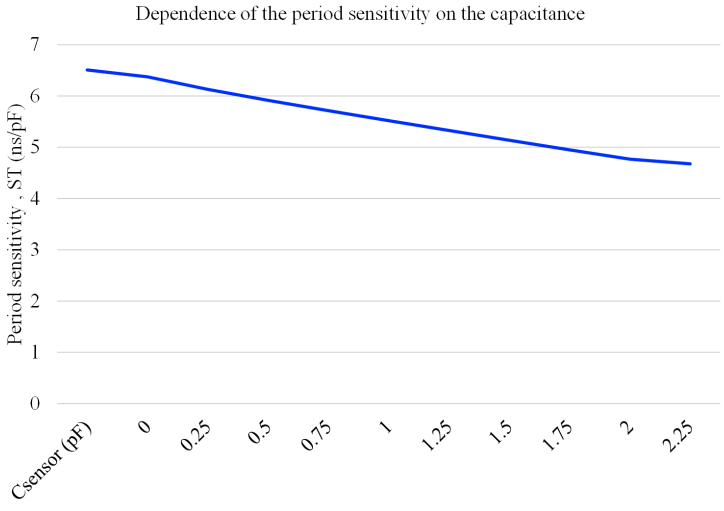

Fig. 2. Dependence of local sensitivity S_T on C_{sensor}

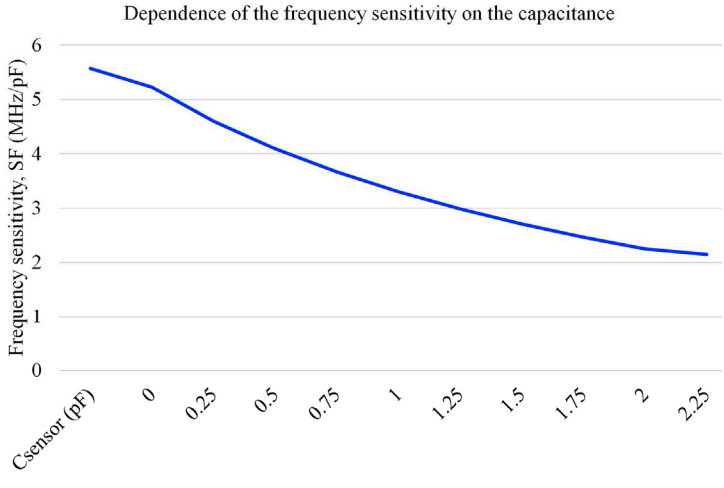

Fig. 3. Dependence of local sensitivity S_F on C_{sensor}

The minimum sensitivity is observed at the maximum value of the capacitance ($C_{sensor} = 2.5$ pF)

$$S_{F,\max} = \frac{\left|F_{step11} - F_{step10}\right|}{C_{step11} - C_{step10}} = \frac{\left|21.17 - 21.71\right|}{0.25} = 2.16\,(\text{MHz/pF}).$$

The calculation showed that the maximum local frequency sensitivity (at $C_{sensor} \approx 0$ pF) is $S_{F,\max} = 5.56$ MHz/pF. Accordingly, the minimum local sensitivity at maximum load ($C_{sensor} \approx 2.5$ pF) was $S_{F,\min} = 2.16$ MHz/pF.

5. 3. Verification of the analytical model by parametric modeling of a ring oscillator with an asymmetric capacitive load

To verify the analytical model represented by formula (3), a comparative analysis of the theoretical calculation (T_{calc}) with the data obtained during simulation modeling (T_{sim}) was carried out. To assess the accuracy of the constructed model, the relative error indicator was chosen, the limit value of which, according to the requirements for precision engineering calculations in microelectronics, should not exceed 2%.

The analytical model is based on the linear approximation $T_{calc}(C_{sensor}) \approx T_0 + S_{T,avg} \cdot C_{sensor}$, where, according to the modeling data, $T_0 = 33.38$ ns and the average sensitivity is $S_{T,avg} \approx 5.54$ ns/pF (calculated between $C = 0$ and $C = 2.5$ pF).

The results of comparing simulation data with linear model predictions, as well as the calculation of absolute and relative errors, are given in Table 2.

The data in Table 2 demonstrate a high correlation of the model with the simulation results (maximum deviation – 1.52%). However, the error is systematic, indicating the presence of minor nonlinearity.

Table 2

Comparison of simulation results T_{sim} and linear calculated analytical model T_{calc}

C_{sensor} (pF)	T_{sim} (ns)	T_{calc} (ns)	Absolute error (ns)	Relative error (%)
0.00	33.38	33.38	0.00	0.00%
0.25	35.00	34.77	0.23	0.67%
0.50	36.56	36.15	0.41	1.12%
0.75	38.07	37.54	0.53	1.40%
1.00	39.52	38.92	0.60	1.52%
1.25	40.92	40.31	0.61	1.50%
1.50	42.28	41.69	0.59	1.40%
1.75	43.59	43.08	0.51	1.18%
2.00	44.85	44.46	0.39	0.87%
2.25	46.06	45.85	0.21	0.47%
2.50	47.23	47.23	0.00	0.00%

5. 4. Energy efficiency assessment of the converter

The key indicators of energy efficiency are the power consumption (P) and the energy consumed per cycle (E_{cycle}). The results of calculating these parameters for the entire range of sensor capacitance are given in Table 3.

As can be seen from Table 3, the average power consumption (P) does not remain constant but shows a slight increase (from 151.3 μW to 155.7 μW) with increasing sensor capacitance.

The energy per cycle (E_{cycle}), which is an integral indicator of quality (Figure of Merit), is calculated as the product of power and period ($E_{cycle} = P \cdot F$). Since the oscillation period (T) increases quasi-linearly, and the power (P) changes insignificantly, the dependence of energy on capacitance has a pronounced quasi-linear character.

Table 3

Energy performance of the converter

C_{sensor} (pF)	Average power consumption, P (μW)	Energy per one cycle, E_{cycle} (pJ)
0	151.31	5
0.25	151.46	5.3
0.5	151.87	5.55
0.75	152.38	5.8
1	152.98	6
1.25	153.53	6.28
1.5	154.09	6.52
1.75	154.57	6.74
2	155.08	6.96
2.25	155.4	7.16
2.5	155.67	7.35

In the studied range, the energy consumption per measurement increases from 5.05 pJ (at $C_{sensor} = 0$) to 7.35 pJ (at $C_{sensor} = 2.5$ pF). Our results indicate that dynamic energy consumption is dominant, and its linear dependence on capacitance allows one to easily predict the energy budget of the system during design.

6. Discussion of the result of simulation and analytical model of an asymmetric ring oscillator

The obtained results allow us to formulate several key conclusions regarding the design of capacitance-to-frequency converters based on asymmetric ring oscillators.

The constructed model $T_{osc}(C_{sensor}) \approx T_0 + S_T \cdot C_{sensor}$ showed high accuracy (relative error < 2%). This is explained by the fact that it is based on the correct physical principle of adding delays of asymmetric cascades (1), and the linear approximation of the delay in formula (2) is a sufficiently accurate approximation for engineering calculations. The insignificant nonlinearity T_{sim} (Table 2) is associated with second-order effects, such as degradation of the output voltage rise rate due to asymmetry [24] and the nonlinearity of the alpha power law [19], which is characteristic of 45-nm technology.

The detected nonlinearity of the sensitivity of the frequency change (a drop from 5.57 to 2.15 MHz/pF) is a direct mathematical consequence of the hyperbolic characteristic of the capacitance-to-frequency conversion (4). This means that the frequency change at the same increments of the sensor capacitance occurs unevenly over the entire measurement range. The practical consequence of this is that the resolution of the measuring system will be significantly higher in the region of small capacitance values (where the sensitivity reaches 5.56 MHz/pF) and will decrease when approaching the upper limit of the dynamic range. Such non-uniformity complicates accurate calibration and interpretation of the results without additional linearization. That is why, to obtain a linear measurement, the digital part of the system should measure not the frequency, but the period T_{osc} since it is it (Table 2) that has a quasi-linear dependence on the sensor capacitance.

The key result is the confirmation of the linear dependence of E_{cycle} on the sensor capacitance (Table 3) with a slope close to VDD^2. This provides a powerful design tool: the energy cost of one cycle measurement is $E_{cycle,0}$ (base cost) plus $C_{sensor} \cdot VDD^2$ (measurement cost).

Unlike [17], in which an ultra-high sensitivity of 180 aF is achieved, this study focuses on the 2.5 pF range, which is typical for many MEMS sensors (e.g. accelerometers) [3]. This is made possible by the direct and simple integration of the sensor into the ring oscillator circuit.

In contrast to study [8], which also uses a 45 nm ring oscillator, our study proposes and validates a simple analytical model (3) suitable for design, rather than just sampling simulation data.

Unlike study [1], in which the consumption of 10.23 μW at 65 nm was achieved, the consumption in this study is significantly higher (about 155 μW). This is explained not by the technology but by the design decision: the use of large fixed capacitive loads $C_{load} = 1$ pF on each stage. Despite the increase in power, this approach makes practical sense because it makes the base frequency less sensitive to parasitic capacitance and process variations [11], stabilizing the initial operating point of the converter. In addition, a slight increase in the average power consumption is observed with increasing sensor capacitance. This phenomenon is explained by the change in dynamic losses when the operating frequency decreases.

The proposed and tested model (3), (4) directly solves the problem of the lack of a simple tool for describing an asymmetric loaded ring oscillator. It makes it possible to predict the characteristic of capacitance-to-frequency conversion with an error of less than 1.55% (Table 2), which is sufficient for primary engineering design.

Our study has certain limitations. In particular, the proposed model (3), (4) is semi-empirical in nature since the coefficients T_0 and S_T are obtained from simulation and not derived from the parameters of the alpha power law [25]. In addition, the modeling was carried out for idealized conditions (nominal parameters of the technological process, fixed temperature) without taking into account the spread of parameters.

Among the shortcomings of the proposed technical solution, it is worth noting the sensitivity of the single-cycle circuit to interference, which is manifested in the low noise suppression coefficient of the power source and is critical for real operating conditions. Another aspect is the compromise of energy efficiency. The use of large load capacitances C_{load} for delay linearization leads to increased energy consumption compared to solutions based on inverters with minimal dimensions.

In the future, the disadvantages described above can be eliminated by modifying circuit solutions. In particular, to level the sensitivity to interference and power noise, one can switch to a differential ring oscillator topology [17]. The issue of increased energy consumption is advisable to solve by optimizing the "stability-power" trade-off, reducing the load capacitance of cascades C_{load} (for example, to 10–50 fF).

7. Conclusions

1. An analytical model has been proposed that describes the process of converting capacitance into frequency under conditions of asymmetric loading. The mathematical description is based on the physical principle of summing the delays of individual cascades and establishes a relationship between the input variable (sensor capacitance) and the output variable (oscillation period). It is shown that the oscillation period has a quasi-linear dependence on the sensor capacitance, where the constant component is determined by the generator's natural frequency, and the proportionality coefficient depends on the current parameters.

2. The key metrics of the ring oscillator for converting capacitance into frequency have been analyzed. It is established that the characteristic of converting capacitance into frequency has a hyperbolic nature, as a result of which the instantaneous sensitivity is nonlinear and decreases from 5.57 MHz/pF to 2.15 MHz/pF (average 3.52 MHz/pF). Based on this, it is justified that to ensure the linearity of the output characteristic of the measuring system, it is necessary to process the period, not the frequency of the output signal.

3. The proposed model was verified by comparing the calculated data with the results of parametric analysis in the LTspice circuit modeling environment in the capacitance range from 0 to 2.5 pF. The high accuracy of the developed mathematical apparatus was confirmed: the maximum relative error does not exceed 1.55% in the entire operating range, which allows the model to be used for engineering calculations without the need for lengthy simulations.

4. The laws of energy consumption of the converter have been established. It was proven that the energy consumed for

one full oscillation cycle increases linearly with increasing sensor capacitance. It was determined that the growth coefficient of this dependence is numerically equal to the square of the supply voltage, which is formed by the total costs of recharging internal parasitic capacitances, cascade loading, and variable sensor capacitance.

Conflicts of interest

The authors declare that they have no conflicts of interest in relation to the current study, including financial, personal, authorship, or any other, that could affect the study, as well as the results reported in this paper.

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Data availability

The data will be provided upon reasonable request.

Use of artificial intelligence

The authors confirm that they did not use artificial intelligence technologies when creating the current work.

Authors' contributions

Vadym Hula: Conceptualization, Methodology, Validation, Formal analysis, Visualization, Writing – original draft; **Vitalii Vintoniak**: Conceptualization, Methodology, Validation, Formal analysis, Visualization, Writing – original draft; **Volodymyr Hryha**: Validation, Supervision, Writing – review & editing.

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