

Abstract

The developed automated system for vacuum-arc dusting is based on the modern element base and allows the long-term continuous measurement of the arc current, of the residual pressure in the vacuum chamber, of the temperature of parts, of voltage, of the simulation of dusting, as well as determination of the optimal values of controlled parameters and accumulation and storage of measurement results.

During the operation of a vacuum-arc dusting unit, the process parameters and their impact on the quality of coating were studied. The measurement of pressure in the vacuum system of the unit was performed using three vacuum gauges 13BT3-003 and magnetic-discharge locking vacuum gauge ВМБ-14. The countdown of pressure was displayed on a computer monitor and recorded by the universal registration unit with the ADC. Temperature of the surface of details was controlled by a pyrometer BSA with secondary measurement transmitter.

The application of the digital industrial interface RS-485 for connection to a control computer and for data transmission provides increased noise immunity of the entire system. The system architecture is based on standard OPC, which allows the application of measuring modules of different manufacturers.

The automated system allows the measurement of parameters of the vacuum-arc dusting, as well as the calculation of the parameters of the process and generation of the appropriate control influences by modes of dusting

Keywords: vacuum-arc dusting, coating, standard OPC, SCADA

Друкowana плата – це пластина з діелектрика, на якій з'єднані між собою компоненти електронних приладів. Один з кінцевих етапів виробничого процесу – забезпечення покриття поверхні відкритих частин плати. Покриття поверхні відіграє важливу роль з двох причин: воно захищає мідне покриття підкладки від корозії, а також створює поверхню, до якої припадають компоненти наступних етапів складання

Ключові слова: покриття поверхні, друкowana плата, вирівнювання припою гарячим повітрям, імерсійне золочення по підшару нікеля, органічне захисне покриття

Печатная плата – это пластина из диэлектрика, на которой соединяют между собой компоненты электронных приборов. Один из конечных этапов производственного процесса – обеспечение покрытия поверхности открытых частей платы. Покрытие поверхности играет важную роль по двум причинам: оно защищает медное покрытие подложки от коррозии, а также создает поверхность, к которой припаиваются компоненты следующих этапов сборки

Ключевые слова: покрытие поверхности, печатная плата, выравнивание припоя горячим воздухом, иммерсионное золочение по подслою никеля, органическое защитное покрытие

УДК 004.89

COMPARATIVE ANALYSIS OF SURFACE FINISHES OF PRINTED CIRCUIT BOARDS

Partinova Simona
PhD Student
Faculty of Electronic Engineering and Technologies,
Technical University - Sofia,
8 Kliment Ohridski Blvd.
1000 Sofia, Bulgaria,
E- mail: simona34@abv.bg

1. Introduction

Surface finishes on printed circuit boards are applied in the production process of PCBs to pads and other elements of the outer layers, not covered with protective mask.

Purpose of the application of such finishes is to provide adequate soldering surface for assembly on the PCB copper layers and to protect from oxidation and wear.

The choice of an appropriate finish is determined by the technology of assembly in the process of population of bare boards and main parameters for such choice are solderability and finish's compatibility with the solder paste. If this finish is subject to mechanical damage, one must carefully select its coefficient of friction, wear resistance, and mechanical strength. When there are

pads and other non-covered electrically conductive areas that would provide for various functions on a single board, various finishes can be applied, or only one as a compromise in regard to reliability.

There is a number of standards that define surface finishes and among most important of them are:

- J-STD-003 "Solderability Tests for Printed Boards": This standard prescribes test methods, defect definitions and illustrations for assessing the Solderability of printed board surface conductors, attachment lands, and plated-through holes; [1]
- IPC 2221 "Generic Standard on Printed Board Design": This standard is intended to provide information on the generic requirements for printed board design. [2];

- IPC-7095A “Design and Assembly Process Implementation for BGAs”: focuses attention on the design of PCBs using BGA packages [3].

In summary, the main purpose of surface finishes is to protect the copper surface of the pads from oxidation and wear, and to provide high quality soldering of electronic components. This purpose leads to the following requirements: good material coverage with a solder paste, long life of solderability, good resistivity to moisture.

Main materials used for surface finishes are metals and their alloys. The only exception is OSP which is special not only because it is organic, but also because of his ability to dissolve and form a bond in the process of soldering.

The following five surface finishes are considered as the most popular at the present moment:

2. HASL (Hot Air Solder Leveling)

Tin-lead HASL has been the standard surface finishing method used in the manufacture of double-sided and multi-layer boards due to its excellent solderability during assembly.

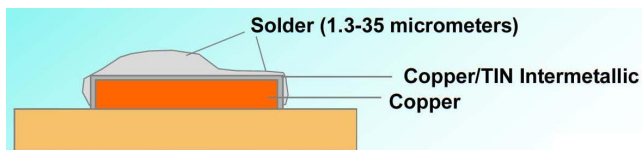


Fig. 1. Tin-lead HASL

Until recently, this type of finish was primarily used in the covering of printed circuit boards due to the excellent performance of the soldering tin-lead alloy and its relatively low price. Recently it lost its relevance because of increasing use of lead-free boards and because of increasing demands on the density and size of the contact pads for components.

As a result of this process pads are covered with eutectic alloy layer of lead and tin.

Typical coating thickness specifications are:

- 2.5µm to 25µm with an average;
- 1.3µm to 2.5µm on discrete pads (average around 2µm);
- 3.8µm to 10µm coverage on large surface like ground plane. [4]

During the HASL process, solder mask-coated boards are first cleaned and etched to prepare the contact surfaces for the solder. Following the application of flux to a board, a layer of solder is applied to the copper surfaces by submersing the panel in molten solder. The excess solder is then blown away from the board by an air knife, leaving a thin, protective layer of solder on the exposed circuitry. [5]

The process can be operated either in a horizontal, conveyorized mode, or in a vertical, non-conveyorized system. During vertical mode process the panel is immersed vertically in molten solder at a temperature of ~ 260° C, then rapidly removed and any redundant solder is removed with a blow coming from hot air jets known as "air knife".

Finishes of pads with an orientation different from the airflow are with different thickness: those perpendicular to the "air knife" are thinner than those parallel to it, as the airflow blows board's plane at 90° angle. In this process, the bottom of the board remains in the bath of molten solder for 4-5 seconds longer than the nominal time, but this acceler-

ates the diffusion of copper and can lead to contamination of the solder. Usually this method is applied only for boards that do not provide for SMT components placement. [6]

During the horizontal mode tinning process, as the boards move along conveyor and passes through the solder bath, then it is blown with air jet. Uniform thickness of coating is provided here by the location of the conveyor plate and the hot air knife angle of 45°.

Flux selection is critical to the result of this process. The flux is responsible for creating the surface conditions required to achieve a high quality solder deposit on the PCB. Fluxes are available in a variety of formulations with differing characteristics such as viscosity, foam level, acidity, volatile content, and type of activator. The type of HASL flux ultimately selected will depend on the type of chemicals and processes used in previous manufacturing stages, on the type of solder mask, and the solder deposit characteristics required.

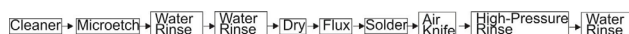


Fig.2 Horizontal mode tinning process

The main advantages of this process are excellent solderability, low price, and long shelf life.

A major disadvantage of the HASL surface finish however is its varying thickness and non-flat pads caused by the accumulation of solder, especially on large metal areas. Using HASL is not recommended when designed board contains components smaller than 0603. [7]

The HASL process in non- RoHS compliant.

3. Electroless Nickel/Immersion Gold (ENIG)

The Electroless Nickel/Immersion Gold finish consists of a relatively thick layer of nickel (1-8 µm) followed by a thin (~ 0,05–0,2 µm) protective layer of gold.

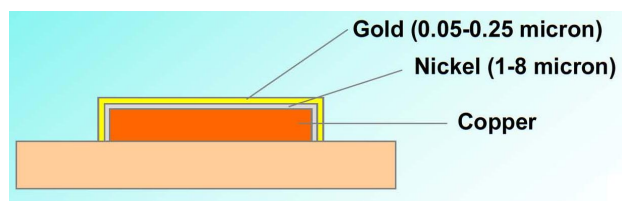


Fig.3 The Electroless Nickel/Immersion Gold finish

The Nickel/Gold process is applied through the deposition of an initial layer of nickel followed by a thin, protective layer of gold, onto the exposed copper surfaces of a PCB. Nickel characteristics such as hardness, wear resistance, solderability, and uniformity of the deposit make this a desirable surface finish. The thin layer of immersion gold preserves the solderability of the finish by preventing oxidation of the highly active nickel surface. Nickel/Gold finishes typically can withstand thermal excursions (heating cycles) without losing solderability.

Immersion gold can be applied to cleaned copper or to a previously applied sub-layer of nickel. Nickel-plating is done in slightly acidic solution that allows the deposit of corrosion-resistant alloy of nickel and phosphorus (8-10% phosphorus). Tin-less grainy and low-porous layer of gold applied to the surface provides good solderability and

protects nickel from oxidation. The nickel serves as a barrier between the gold and copper at preventing their mutual diffusion and subsequent oxidation of copper.

After the application of ENIG, the use of an organic flux or such one that does not require washing after soldering is recommended.

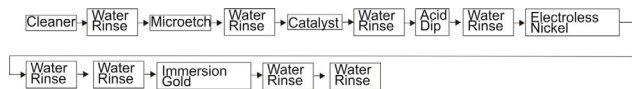


Fig.4. The Nickel/Gold process

The process is performed in a vertical, non-conveyorized mode which reduces productivity and increases production cost.

The application of gold over nickel-plated surface is possible due to the controlled oxidation of nickel (exchange reaction). Due to the difficulty in controlling corrosion of nickel, corrosion could penetrate deeper and closer to the copper layer. This should create problems with solderability and durability at the solder joint. As shown in tests done on BGA packages, solders based on tin-lead alloy and applied onto a copper surface are more resistant and stable than solders based on nickel compounds [8].

Due to the different coefficients of thermal expansion, especially when working with large sizes packages can be obtained stress in solder joints, which can destroys the solder joints. The designer selects the PCB material should bear this in mind that if the device contains BGA or other large component size, the nickel layers should be avoided.

- The main advantages of this finish are:
- Excellent corrosion resistance;
- Good for aluminum wire bonding;
- Excellent flatness for fine-pitch technology;
- Excellent solderability;
- Excellent shelf life.

It should be noted that most materials applied by chemical or electrochemical method is suitable for lead-free soldering, thereby meeting the RoHS Directive. But a major disadvantage is that the condition of high temperature and humidity makes solder joints easily destroyable.

The most common defects observed in the PCB, using ENIG process is the formation of porous gold-plating, “fragile” failures on large BGA packages, extraneous nickel plating and the effect of gold called “black pads” which is brittle solder joints.

The formation of a porous layer of finish takes place when the gold atoms do not form a solid crystal lattice, thereby allowing nickel atoms to migrate and reduce the quality of solder joints.

“Fragile gold” occurs when in the outside copper layers of the board are dissolved large amounts of gold, which forms brittle intermetallic compound AuSn₄, at which borders solder joints are easily broken. This usually can be controlled by maintaining level of gold in binder not to exceed 4% by weight and thickness should not be greater than 0,064 μm. The way to avoid this problem is reported in standard J-STD-001. When a component with leads covered with Sn/Au alloy is to be soldered, the technological process of board assembly must include a preliminary step before soldering - dipping component’s leads in solders until partial dissolution of gold.

The problem was first identified on BGA components. An open or fractured solder joint sometimes occasionally

appears after board assembly on a BGA pad. The solder had wet and dissolved the gold and formed a weak intermetallic bond to the nickel. This weak bond to the nickel readily fractures under stress or shock, leaving an open circuit. The incidence of this problem appears to be very sporadic and a low ppm-level problem, and its occurrence has been very unpredictable. The problem has occurred on solder joints of other types of components, such as QFP’s. In spite of their dissimilar features, leads on the QFP components, the solder joint does not experience the same stress as on BGA joints, but defect can still occur. The solder joints can be touched-up without removing the component and the defect may not manifest. A BGA solder joint cannot be touched-up without the component being removed. After the BGA component is removed, a ‘black pad’ is observed at the affected pad site. This black pad is not readily solderable, but it can be repaired. “Black pads” defect appears to occur more frequently on boards on finer pitched components with smaller pads, than on larger pads. [9]

Unfortunately, the mechanisms leading to this defect are not adequately studied, but studies show that it occurs in the presence of residual phosphorus in the galvanizing bath.

According to an article by Dewey Benson, published in the journal “Solid State Technology” [9], the use of limited soldermask is recommended in the design of boards with BGA components (non solder mask defined pads - NSMD).

4. Immersion Silver (ImAg)

The Immersion Silver finish consists of a silver layer and a protective organic coating.

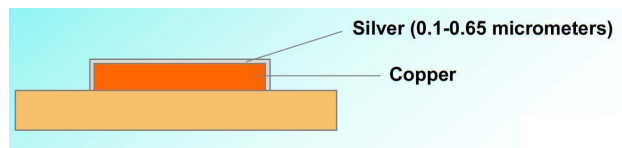


Fig.5. Immersion silver finish

The Immersion Silver finish is produced by the selective displacement of copper atoms with silver atoms on the exposed metal surface of the PCB. To minimize silver tarnishing, an organic inhibitor is co-deposited to form a hydrophobic layer on top of the silver.

Technology consists of double pre-cleaning and a silver bath. To prevent migration of silver on the PCB, silver is applied together with an organic compound, which not only protects it from migrating, but also from oxidation as it plays the role of antioxidant preservative coating.

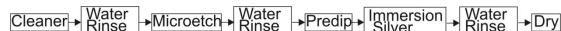


Fig. 6. The Immersion Silver finish process

The thickness of the silver coating is usually in the range 0,08 to 0,65 μm, which is achieved by keeping the board in a silver bath for 1-4 minutes. The small thickness of this finish decreases production costs. In the process of placing components on the board, silver completely dissolves in solder paste creating homogeneous alloy of Sn/Pb/Ag directly onto copper surface, which gives very good solder reliability, including when soldering BGA components. [10]

The reliability of this finish exceeds that of the OSP, but is lesser than that of ENIG.

During their storage and use, already assembled boards can acquire a yellowish tinge, which is the result of environment pollution with sulfates or chlorides. This does not affect boards' properties.

The main advantages of Immersion Silver finish are:

- Excellent flatness for assembling components with fine-pitch technology;
- Do not contains nikel;
- High Stability;
- Long shelf life;
- Process control simplicity;
- Replenishable Reduced make-up costs.

The disadvantages are high coefficient of friction and discoloration due to reaction with sulfur in the air which doesn't impact solderability.

5. Immersion Tin (ImSn)

The Immersion Tin finish displaces surface copper.

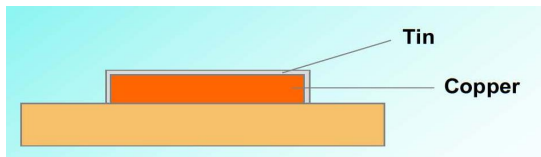


Fig.7. The Immersion Tin finish

The Immersion Tin process utilizes a displacement reaction between the board's copper surface and stannous ions solution to reduce a layer of tin onto the copper surfaces of the PCB. The process may use a conveyorized system or it may be used in a vertical, non-conveyorized mode. Immersion Tin surfaces are compatible with SMT, flip chip, BGA technologies, and typical through-hole components, but it is not a wire-bondable finish.

There are a number of different Immersion Tin systems available, including those based on methane sulfonic acid, sulfate, chloride, and fluoborate compounds. Tin surfaces are compatible with all solder masks, have a shelf life of at least one year, and can typically withstand a minimum of five thermal excursions during assembly.

The process of applying immersion tin is another alternative to HASL and it is a process similar to those used in finishes with immersion silver, with the exception of the long residence time in the bath (about 10-15 minutes). We also conducted additional cleansing to flush away tinned electrolytes. Same as with the case of bath used with ENIG plating process, so is the bath for tin-plating an unfavorable environment for a protective mask on the PCB, so the process of applying these masks should be the last application of immersion tin. Layer thickness is in the range 0,6 - 1,5 μm. There is need to perform tests for solderability of the finish. The tin is a good soldering surface for SMT components, but the amount of heating cycles should be limited. The duration of the process of applying immersion tin is about 35 minutes.

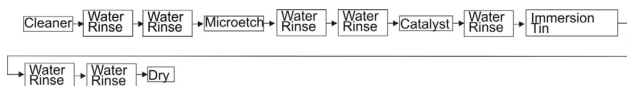


Fig. 8. The Immersion Tin process

The tin used as finish is characterized with two main issues: the formation of so-called "whiskers" of tin and the ability to form intermetallic layers which grows with time and heat cycles.

Tin "whiskers" (length 150 μm) are thin crystal fibers, which can provoke occurrence of bridges on electrical board layers. The process of formation has not been completely studied and there is no simple answer to the question about their origin or how to prevent their occurrence. It could be said that the main cause for whiskers appearance is increased tension in the layer of tin, which occurs as the result from the formation of intermetallic structures, oxidation, and corrosion, cyclic changes in temperature or mechanical stress. [11]

The formation of intermetallic compounds such as Cu_xSn_y can cause worsening solderability. Usually, into the solder joints, intermetallic layers act as a mechanical connection, but since the thickness of the tin coating is not greater than 1,5 μm, in the formation of these compounds, this thin layer is rapidly absorbed. To avoid these disadvantages, a technology for the application of different barrier underlayers, such as metalloorganic is used. These underlayer burn during soldering.

Other serious problems are limited capability of high density boards and limited endurance to multiple assembly/disassembly of components.

6. Organic Solderability Preservative (OSP)

The OSP finish is an organic (non-metallic) film that bonds to exposed copper.

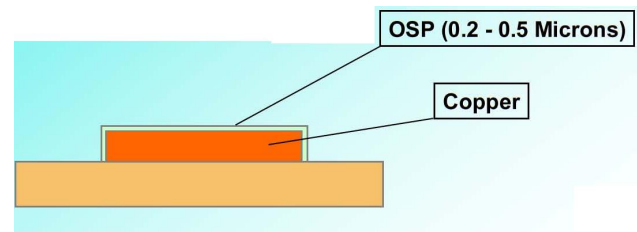


Fig.9. The OSP finish

The OSP finish is an anti-oxidant film applied to exposed copper surfaces that reacts with copper to form an organometallic layer. This coating is nearly invisible, and may be applied either as a thick benzimidazole (4 to 20 microinches / 0.1 to 0.5 microns) or thin imidazole [monomolecular (30 to 100 angstroms)] layer.

OSP, consisting of an organic layer located on the copper surface of the outside layers of the boards and protecting them from oxidation are used as an alternative to metal finishes. [12]

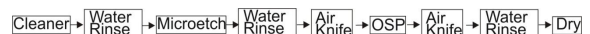


Fig. 10. The OSP process

The OSP process typically is operated in a horizontal, conveyorized mode but can be modified to run in a vertical, non-conveyorized mode. OSP processes are compatible with SMT, flip chip, and BGA technologies, and with typical through-hole components, but the OSP finish

cannot be wirebonded. OSP surfaces are compatible with all soldermasks and have a shelf life of up to one year.

The advantages of this finish are:

- Lower cost.
- Reduced safety and environmental concerns;
- No board warp or twist. Higher yields;
- Process/thickness control. Higher yields;
- Applicable to a wide range of assembly requirements;

Fast, economical installation. Multiple Final Finish capability in a single line.

This finish has some disadvantages though, such as degradation at high temperature and because of this, limited amount of solder cycles; sensitivity to improper storage and transportation (can be easily scratched, and is sensitive to fingerprints), limited choice of flux, sensitivity to solvents used to clean the boards in case of incorrect application of the binder paste (alcohol-based solvent wash off 75% of the coverage, while those based on water wash off 15%).

Reference

1. Standart: J-STD-003 "Solderability Tests for Printed Boards";
2. Standart IPC 2221 "Generic Standard on Printed Board Design";
3. Standart IPC-7095A "Design and Assembly Process Implementation for BGAs" ;
4. "Alternative Technologies for Surface Finishing" Pollution Prevention Information Clearinghouse and U.S. Environmental Protection Agency, website: www.epa.gov/opptintr/library/ppicdist.htm
5. Beauvillier, Luc; Holle Galyon; Matt Stevenson; Darren Hitchcock – "PWB Surface Finishes" –SMTA Meeting, March 16th, 2005;
6. Kermit Aguayo. "Selection of PWB finish" - Process Sciences Inc., 2008
7. Beauvillier, Luc – "The Quest for the Ultimate Surface Finish". Published in "Printed Circuit Design" magazine; Jun 2002, Vol. 19, Issue 6, p 27;
8. F. D. Bruce Houghton. "Solving the ENIG Black Pad Problem: An ITRI Report on Round 2" PWBRRC;
9. Duane Benson. "Black Pad – And Then Some SMT", smt.pennnet.com;
10. "The Quest for the Ultimate Surface Finish", printed circuit design – June, 2002. www.merix.com;
11. "Surface Finish Options" Merix Corporation. www.merix.com;
12. Solberg, Vern. "Specifying Base Materials for SMT Circuit Boards", Part 3 SMT – September, 2005

Abstract

This article describes surface finishes which are the most common and well-established at present time at the assembly operations of electronic products. The process of further improvement of these finishes is continuing, and actively develops unlike their less common counterparts - different finishes based on palladium and galvanically deposited NiSn and SnAg finishes. Outside of the scope of this article remain important issues, such as a detailed examination of a number of lead-free coatings and methods for solderability testing, measuring the surface resistance of the coating and the shear strength of solder joints in compliance with international standards. These issues will be covered in future articles on these subjects.

Key words: surface finishes, PCB, HASL, ENIG, OSP

ОТ АВТОРА

Я, Лебедев Владимир Владимирович, автор статьи "Ударопрочные композиции на основе полидициклопентадиена", опубликованной в «Восточно-Европейском журнале передовых технологий» №5/10(59) (с. 21-23) приношу свои извинения Аширову Роману Викторовичу (Национальный исследовательский Томский политехнический университет, Россия) в связи с тем, что в названной статье не было указано его авторство в отношении результатов экспериментальных данных. Прошу считать этот факт недостаточной внимательностью при подготовке мною статьи для опубликования.

Прошу рассмотреть возможность подачи статьи в новой редакции, после согласования мною всех неучтенных аспектов с Ашировым Романом Викторовичем - представителем коллектива учёных Национального исследовательского Томского политехнического университета, принимавших участие в проведении экспериментальных работ и получении результатов экспериментов, приведенных в опубликованной статье.