ISSN 2664-9969

UDC 621.314
DOI: 10.15587/2706-5448.2020.207893

Zheliazkov Y.

RESEARCHING THE EFFICIENCY OF BUCK CONVERTER SYNCHRONOUS RECTIFIER

The object of study is synchronous buck-voltage converter with digital control system. One of the most problematic things is energy changing and transmission in converters to reach certain numerical range with minimal losses in the components of the electrical circuit. An enormous calculated parameters of electrical scheme. There was advised and described both structure and electrical scheme of synchronous converter, which, thanks to digital system, provides dates with more accuracy connected with an impact on working scheme. There was shown detailed analysis example with a numerical value for the certain elements of electrical scheme. It's a fundament in order to choose certain parts of electrical scheme according to the certain categories.

During research there was used selection of hardware and software tools: elements for buck-converter – key, diode and capacitor; certain voltage and frequency range for microcontroller; control of the power keys of the circuit with the corresponding operating parameters for driver. There was analyzed and calculated all over the possible losses during the process bucking of the voltage to the certain level, an enormous losses in the components of the converter electrical scheme – induction coil, keys and capacitors. It's an important part of synchronous buck-converter. There was calculated power losses and efficiency through the received graphics of keys commutation in electrical scheme. There were received graphic dependence of converter efficiency on output power; time characteristics of the control signal pulse-width modulation (PWM) and output voltage; dependence on the commutation losses. This is because advised synchronous converter has a set of features. Particularly analog to digital converter in the capacity of feedback, digital regulation system with a discrete step and rectification by replacing diodes with actively controlled switches. There are keys of low-side and high-side levels according to the passing voltage and current values. Therewith provides possibility for receiving more accuracy value. In comparison with analogic buck-converters, this converter has voltage parameter with fractional error.

Keywords: *buck converter, digital control, buck converter losses, buck-converter efficiency, synchronous rectifier.*

Received date: 15.03.2020
Accepted date: 17.05.2020
Published date: 31.08.2020

1. Introduction

Nowadays energy efficient projects are becoming more popular. An enormous converter, which can be used in photovoltaic power generation systems, renewable energy systems and a number of other systems. For example, modern aircraft use a lot of radio equipment for communication systems, navigation, landing, meteorological, avoiding the collision of aircrafts. For obvious reasons, the weight and volume of this equipment must be reduced. The traditional construction scheme uses one powerful transmitter and a number of switched antennas or antenna array. In addition, there is a constant integration of equipment in the direction of combining several systems within a single functional unit [1]. At the same time, of course, the weight and dimensions are reduced, but additional requirements are imposed on the element base.

Modern equipment is characterized by a high complexity. Device requires different voltages in order to supply its own component parts [2].

When there is electric power supply in order to use different voltage steps, it is important to use special converters (regulators). The problem for receiving different voltage supply values is in portable equipment.

There is in mains-powered devices can be build an electric power supply with the required voltage. By the way portable devices operate from stand-alone power sources and certain voltage stages can be received by using *DC / DC* (*DC* means direct current) converters.

Requirement in order to receive huge coefficient of efficiency is important for devices with a stand-alone power sources.

It is relevant to study the existing schemes of energy converter and carry out a comparative analysis, because the buck converters use the active modes for switching [3]. Thus, *the object of research* is synchronous buck converter with digital control system. *The aim of the article* is the researching of the scheme and developing the foundations for construction in order to reach high efficiency level of buck converter.

2. Methods of research

2.1. Engineering analysis of buck converter. There is in Fig. 1 an electrical principle scheme of the buck voltage converter. Power circuit of converter has transistor VT_1. If the key switched on, output current, which flows through the inductance coil (L), rises. Inductance coil is coupling magnetic field energy. If the key switched off, coupled electrical energy in the inductance coil will be send to the capacitor (C) and load (R_L). Bypass diode (VD_1) lets the pass for the current to flow.

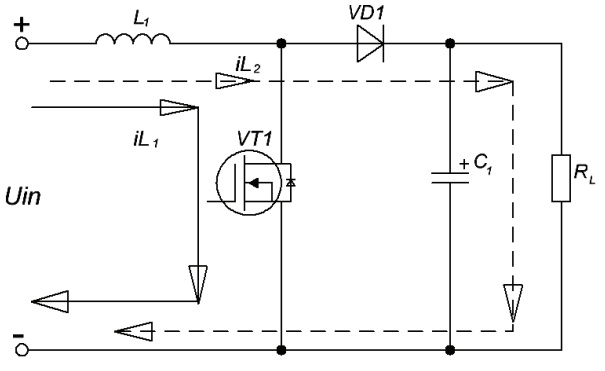


Fig. 1. Scheme of the buck converter

In order to realize the scheme it is important to calculate nominals of the elements in the buck converter [4, 5]. Calculation would be finished with a certain parameters: maximal output current $I_{out.\max} = 0.522$ A, frequency switching $f_{sw} = 10$ kHz, inductive current ripple factor $LIR = 0.3$, range of input voltage $U_{in} = 7 - 24$ V and output voltage $U_{out} = 6$ V [6].

Inductance calculation is an important moment during converter projecting, insofar as there is dependence on values of maximal input $U_{in.\max}$ and output U_{out} voltage:

$$L = (U_{in.\max} - U_{out}) \frac{U_{out}}{U_{in.\max}} \frac{1}{f_{sw}} \frac{1}{LIR \cdot I_{out.\max}},$$

$$L = (24-6)\ \text{V} \frac{6\ \text{V}}{24\ \text{V}} \frac{1}{10^4\ \text{Hz}} \frac{1}{0.3 \cdot 0.522} = 2.87\ \text{mH},$$

where f_{sw} – frequency switching transistor; LIR – inductive current ripple factor; $I_{out.\max}$ – maximal value of output current.

Peak current of the inductance coil I_{peak} solves as:

$$I_{peak} = I_{out.\max} + \frac{\Delta I_{ind}}{2},$$

$$I_{peak} = 0.522\ \text{A} + \frac{0.3 \cdot 0.522}{2} = 0.6\ \text{A},$$

where $\Delta I_{ind} = LIR \cdot I_{out.\max}$ – variable inductance value.

Output capacitor with a maximum available amplitude swing of ripples of the output voltage ΔU (accept $\Delta U = 100$ mV):

$$C_{out} = \frac{L}{(\Delta U + U_{out})^2 - U_{out}^2} \left(I_{\text{out.max}} + \frac{\Delta I_{ind.}}{2} \right),$$

$$C_{out} = \frac{2.87\ \text{mH}}{(100\ \text{mV}+6)^2 - 6^2} \left(0.522 + \frac{0.1566}{2} \right)^2 = 0.8\ \text{mF}.$$

Capacitance of the input capacitor, including of the load current I_L and swing of ripples of the output voltage $U_{out.ripple}$:

$$C_{out} = \frac{I_L}{2\pi f_{sw} U_{out.ripple}},$$

$$C_{in} = \frac{0.522\ \text{A}}{2 \cdot 3.14 \cdot 10^4\ \text{Hz} \cdot 40\ \text{mV}} = 207.8\ \text{uF}.$$

Duty cycle of the open state power key relative period of the pulse width modulation:

$$D = \frac{U_{out}}{U_{in}} = \frac{6\ V}{12\ V} = 0.5 = 50\ \%.$$

2.2. Synchronous rectifier. Pulse regulators are known as highly efficient power supplies. In order to increase their efficiency, it is important to understand the basic mechanism of power loss. This instruction for use explains the coefficients of electricity losses and methods of their calculation. This also explains how the relative importance of power loss factors depends on the switching power supply specifications [2].

Fig. 2 shows a block diagram of a synchronous rectifier type of DC/DC (DC means «direct current») converter. Fig. 3 shows the waveform of the voltage node of the switch and the current waveform of the inductor. Striped lines are areas where losses can be explained.

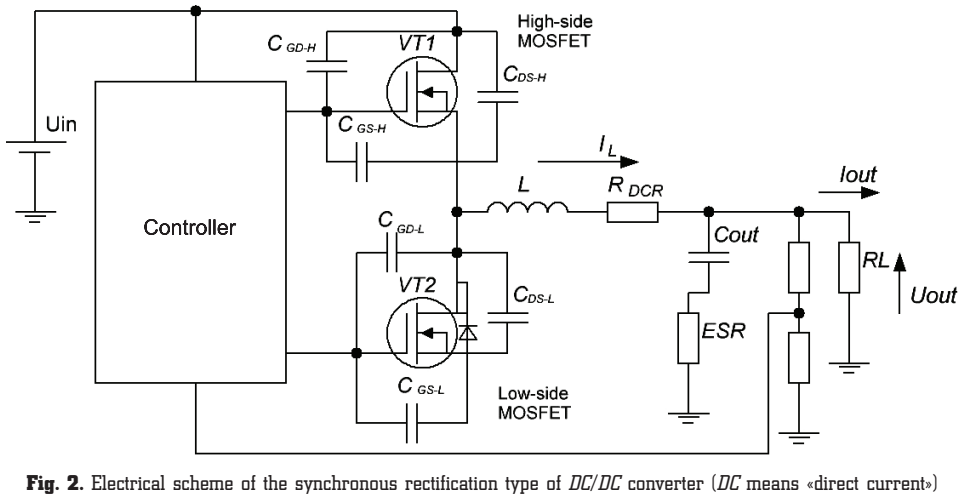


Fig. 2. Electrical scheme of the synchronous rectification type of *DC/DC* converter (*DC* means «direct current»)

ISSN 2664-9969

The following nine factors are the main causes of power loss:

1) conduction losses caused by the on-resistance of the *MOSFET* P_{ON-H}, P_{ON-L};
2) switching-loss in the *MOSFET* P_{SW-H}, P_{SW-L};
3) reverse recovery losses in the body diode P_{diode};
4) output capacitance losses in the *MOSFET* P_{COSS};
5) dead time loss P_D;
6) gate charge losses in the *MOSFET* P_G;
7) operation losses caused by the integrated circuit (IC) control circuit P_{IC};
8) conduction losses in the inductor $P_{L(DCR)}$;
9) losses in the capacitor $P_{C(in)}$, $P_{C(out)}$.

2.3. Buck converter losses

2.3.1. Conduction loss in the MOSFET. The conduction loss in the *MOSFET* is calculated in the A and B sections of the waveform in Fig. 3. As the high-side *MOSFET* is ON and the low-side *MOSFET* is OFF in the A section, the conduction loss of the high-side *MOSFET* can be estimated from the output current, on-resistance, and on-duty cycle. As the high-side *MOSFET* is OFF and the low-side *MOSFET* is ON in the B section, the conduction loss of the low-side *MOSFET* can be estimated from the output current, on-resistance, and off-duty cycle.

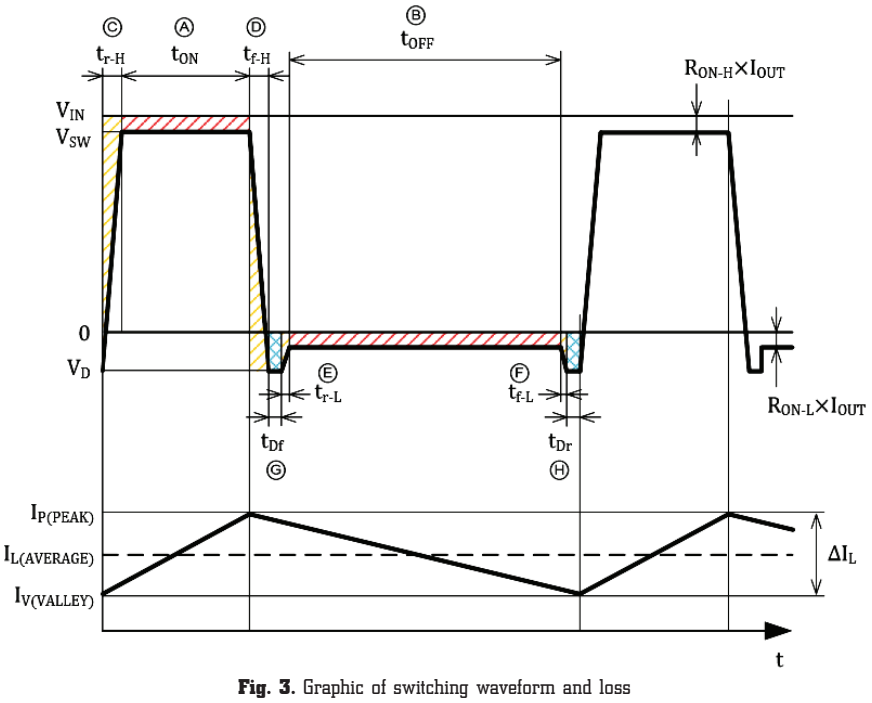


Fig. 3. Graphic of switching waveform and loss

The conduction losses P_{ON-H} and P_{ON-L} could be calculated with the following equations. In this manner, *MOSFET* with a high-side and low-side:

$$P_{ON-H} = I_{out}^2 \cdot R_{ON-H} \cdot \frac{U_{out}}{U_{in}}[W],$$

$$P_{ON-L} = I_{out}^2 \cdot R_{ON-L} \cdot \left(1 - \frac{U_{out}}{U_{in}}\right)[W].$$

According to the last two equations, output current is the average current of the inductor. As shown in the lower part of Fig. 3, greater losses are generated in the actual ramp waveforms. If the current waveform is sharper (peak current is higher), the effective current is obtained by integrating the square of the differential between the peak and bottom values of the current. These losses can be calculated in more detail.

The conduction losses P_{ON-H} and P_{ON-L} are calculated with the following equations:

$$P_{ON-H} = \left[I_{out}^2 + \frac{(I_p - I_V)^2}{12}\right] \cdot R_{ON-H} \cdot \frac{U_{out}}{U_{in}}[W],$$

$$P_{ON-L} = \left[I_{out}^2 + \frac{(I_p - I_V)^2}{12}\right] \cdot R_{ON-L} \cdot \left(1 - \frac{U_{out}}{U_{in}}\right)[W],$$

where

$$\Delta I_L = \frac{(U_{in} - U_{out})}{f_{sw} L} \frac{U_{out}}{U_{in}}$$

is a ripple current of inductor:

$$I_p = I_{out} + \frac{\Delta I_L}{2} \quad \text{or} \quad I_p = I_{out}$$

– current peak of the induction coil; I_V – minimal value of the induction current; f_{sw} – transistor switching frequency; L – inductance value.

2.3.2. Switching-loss in the MOSFET. The switching-losses can be calculated into the «C» and «D» sections or in the «E» and «F» sections of the waveform in Fig. 2. When the high-side and low-side *MOSFET* transistors are turned «ON» and «OFF» alternately, a loss is generated during the transition of the on-switching. Since the equation for calculating the area of the two triangles is similar to the equation for calculating the power losses during the rising and falling transitions, this calculation can be approximated using a simple geometric equation. The switching-loss P_{SW-H} is calculated with the following equation:

$$P_{SW-H} = \frac{1}{2} U_{in} I_{out} (t_{r-H} + t_{f-H}) f_{sw}[W],$$

where t_{r-H} and t_{f-H} are High-side *MOSFET* rise time and High-side *MOSFET* fall time.

When the low-side *MOSFET* is turned ON by the gate voltage while the body diode is energized and then the *FET* is turned OFF by the gate voltage, the load current continues to flow in the same direction through the body diode. Therefore, the drain voltage becomes equal to the forward direction voltage and remains low. Then, the resulting switching-loss P_{SW-L} is very small, as described in the following equation:

$$P_{SW-L} = \frac{1}{2} U_D I_{out} (t_{r-L} + t_{f-L}) f_{sw}[W],$$

where t_{r-L} and t_{f-L} are Low-side *MOSFET* rise time and Low-side *MOSFET* fall time; U_D – forward direction voltage of low-side MOSFET body diode.

2.3.3. Reverse recovery loss in the body diode. When the high-side *MOSFET* is turned «ON», the transition of the body diode of the low-side *MOSFET* from the forward direction to the reverse bias state causes a diode recovery, which in turn generates a reverse recovery loss in the body diode. This loss is determined by the reverse recovery time of the diode t_{RR}. From the reverse recovery properties of the diode, the loss is calculated with the following equation:

$$P_{diode} = U_F \cdot I_{out} \cdot t_{deadtime} \cdot f_{sw}[W],$$

where t_{RR} is a body diode reverse recovery time; I_{RR} is a peak value of body diode reverse recovery current.

2.3.4. Output capacitance loss in the MOSFET. In each switching cycle, the loss is generated because the output capacitances of the high-side and low-side *MOSFET* transistors are charged. This loss is calculated with the following equation:

$$P_{COSS} = \frac{1}{2}(C_{OSS-L} + C_{OSS-H})U_{in}^2 f_{sw}[W],$$

$$C_{OSS-L} = C_{DS-L} + C_{GD-L}, \quad C_{OSS-H} = C_{DS-H} + C_{GD-H},$$

where C_{OSS-L} and C_{OSS-H} are low-side and high-side *MOSFET* output capacitance; C_{DS-L} and C_{DS-H} are low-side and high-side *MOSFET* drain-source capacitance; C_{GD-L} and C_{GD-H} are low-side and high-side *MOSFET* gate-drain capacitance.

2.3.5. Dead time loss. When the high-side and low-side *MOSFET* are turned ON simultaneously, a short circuit occurs between the U_{in} and ground, generating a very large current spike. A period of dead time is provided for turning OFF both of the MOSFETs to prevent such current spikes from occurring, while the inductor current continues to flow. During the dead time, this inductor current flows to the body diode of the low-side *MOSFET*. The dead time loss P_D is calculated in the G and H sections of the waveform in Fig. 2 with the following equation:

$$P_D = U_D I_{out}(t_{Dr} + t_{Df}) f_{sw}[W],$$

where t_{Dr} – dead time for rising; t_{Df} – dead time for falling.

2.3.6. Gate charge loss. The gate charge loss is the power loss caused by charging the gate of the *MOSFET*. The gate charge loss depends on the gate charges (or gate capacitances) of the high-side and low-side *MOSFET* transistors. It is calculated with the following equations:

$$P_G = (Q_{g-H} + Q_{g-L})U_{GS} f_{sw} \quad \text{or} \quad P_G = (C_{GS-H} + C_{GS-L})U_{GS}^2 f_{sw},$$

where U_{GS} – gate drive voltage; Q_{g-H} and Q_{g-L} – gate charge of low-side and high-side *MOSFET*.

2.3.7. Operation loss caused by the integrated circuit. The consumption power used by the IC control circuit P_{IC} is calculated with the following equation:

$$P_{IC} = U_{in} I_{CC},$$

where I_{CC} is integrated current consumption.

The losses in the integrated circuit are caused by excessive temperature, ionizing radiation, mechanical shock and many other reasons. In semiconductor devices, problems in the device package can cause failures due to contamination, mechanical loads on the device.

2.3.8. Conduction loss in the inductor. There are two types of the power loss in the inductor: the conduction loss caused by the resistance and the core loss determined by the magnetic properties. Since the calculation of the core loss is too complex, it is not described in this article. The conduction loss is generated by the *DC* resistance (*DCR*) of the winding that forms the inductor. The *DCR* increases as the wire length increases; on the other hand, it decreases as the wire cross-section increases. If this trend is applied to the inductor parts, the *DCR* increases as the inductance value increases and decreases as the case size increases. Since the inductor is always energized, it is not affected by the duty cycle. Since the power loss is proportional to the square of the current, higher output current results in a greater loss. For this reason, it is important to select the appropriate inductors. The conduction loss of the inductor can be estimated with the following equation:

$$P_{L(DCR)} = I_{out}^2 \cdot DCR.$$

Since the output current is used in this equation, the average current of the inductor is used for the calculation. Similar to the above-mentioned calculation for the conduction loss of the *MOSFET*, the loss can be calculated in more detail by using the ramp waveform for the inductor current calculation:

$$P_{L(DCR)} = \left[I_{out}^2 + \frac{(I_p - I_V)^2}{12} \right] \cdot DCR[W].$$

2.3.9. Loss in the capacitor. Although several losses are generated in the capacitor – including series resistance, leakage, and dielectric loss – these losses are simplified into a general loss model as equivalent series resistance (*ESR*). The power loss in the capacitor is calculated by multiplying the *ESR* by the square of the root-mean-square (*RMS*) value of the *AC* current flowing through the capacitor:

$$P_{CAP(ESR)} = I_{CAP(RMS)}^2 \cdot ESR[W],$$

where $I_{CAP(RMS)}$ is root-mean-square (*RMS*) current of capacitor.

The *RMS* current in the input capacitor is complex, but it can be estimated with the following equation:

$$I_{C_{in}(RMS)} = I_{out} \frac{\sqrt{(U_{in} - U_{out})U_{out}}}{U_{in}}[A].$$

The RMS current in the output capacitor is equal to the RMS value of the ripple current in the inductor, and calculated with the following equation:

$$I_{C_{out}(RMS)} = \frac{\Delta I_L}{2\sqrt{3}},$$

where ΔI_L – ripple current of inductor:

$$\Delta I_L = \frac{(U_{in} - U_{out})}{f_{sw} L} \frac{U_{out}}{U_{in}}[A].$$

ISSN 2664-9969

2.3.10. Total power loss. The power loss of the IC P is obtained by adding all the losses together:

$$P = P_{ON-H} + P_{ON-L} + P_{SW-H} + \\ + P_{SW-L} + P_{diode} + P_{COSS} + P_D + P_G + \\ + P_{IC} + P_{L(DCR)} + P_{C(in)} + P_{C(out)}.$$

Since the total power loss is obtained, the efficiency can be calculated with the following equation:

$$\eta = \frac{U_{out} I_{out}}{U_{out} I_{out} + P}.$$

2.4. Electrical principle scheme of buck converter synchronous rectifier. There is in Fig. 4 a realization of electrical principle scheme of buck converter synchronous rectifier (Fig. 4, *a*) and its implementation in the software application *Proteus* (Fig. 4, *b*). There was taken [7, 8] as a basis. This circuit uses a digital control system, because it maintains a constant output voltage, the controller changes the duty cycle of the control signal, which is directly reflected in the efficiency of the electrical circuit.

For the *MOSFET* in case of high-side voltage was used transistor *IRF*540 and transistor *IRF*540*N* in case of low-side *n*-channel voltage *MOSFET*. It was selected *IR*2184*S* as driver *MOSFET* of the high voltage in the integrated scheme. It can be controlled by the keys in the half-bridge and bridge schemes of the low resistance both with high-side and low-side voltage level. *PIC*16*F*877*A* scheme was used as microcontroller (Fig. 4) [9, 10].

This scheme is very easy to use, coding of this controller is also not difficult. One of the main advantages is that it can be write-erase as many times as possible because it uses *FLASH* memory technology.

3. Research results and discussion

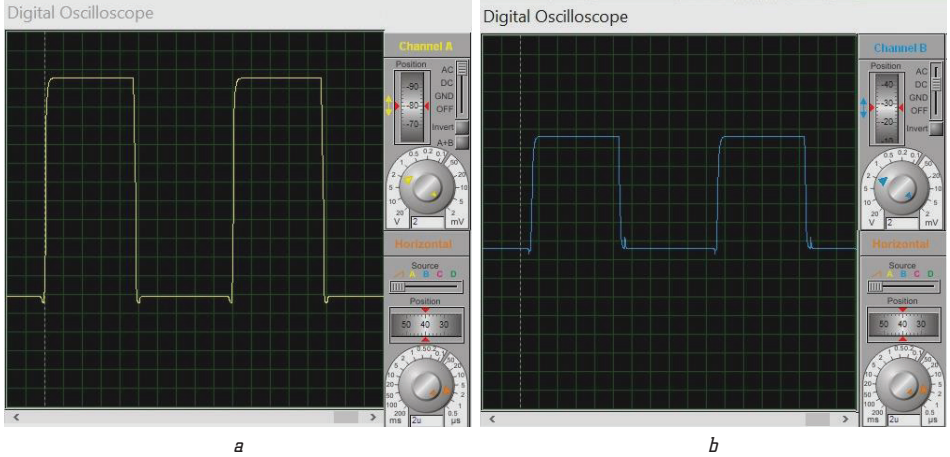
During the simulation of electrical scheme, there were received characteristics in Fig. 5 with the pulse interval for the graphics of the both *MOSFET* transistors $T = 20$ us (20 microseconds).

Fig. 6 shows the switching characteristics of the power switch in the buck converter, which is regulated by the control system, in particular for the field-effect transistor *IRF*540 (*a*) and the power transistor *IRF*540*N* (*b*).

The driver *IR*2184*S* is used as a control system.

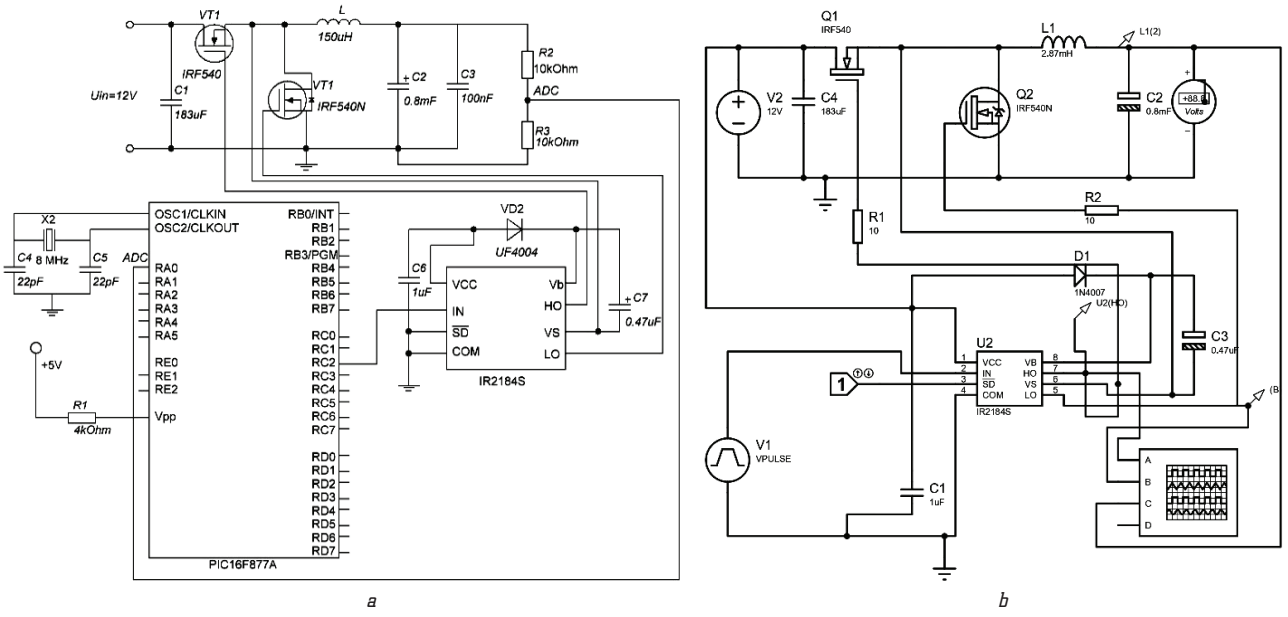
Pulsating value of direct current inductance, where $f_{sw} = 1/20$ us $= 50$ kHz:

$$\Delta I_L = \frac{(U_{in} - U_{out})}{f_{sw} L} \frac{U_{out}}{U_{in}} = \frac{(12\text{ V} - 6\text{ V})}{50\text{ kHz} \cdot 2.87\text{ mH}} \frac{6\text{ V}}{12\text{ V}} = 21\text{ mA}.$$



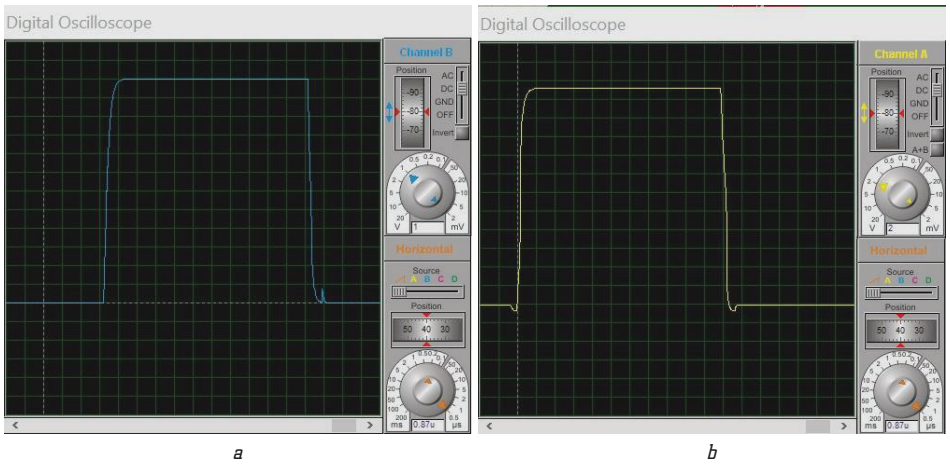
a *b*

Fig. 5. Switching graphics in electrical scheme:
a – for *FET IRF*540; *b* – for *n*-channel *MOSFET* transistor *IRF*540*N*



a *b*

Fig. 4. Electrical schematic diagram of the buck converter:
a – with the synchronization scheme; *b* – with an implementation in the software application *Proteus*



a *b*

Fig. 6. Switching graphs in the electrical circuit with numerical pulse parameters: *a* – for the field-effect transistor *IRF*540; *b* – for the *n*-channel power *MOSFET*-transistor *IRF*540*N*

Peak value of induction current:

$$I_p = I_{out} + \frac{\Delta I_L}{2} = 0.011\ \text{A} + \frac{21\ \text{m}}{2} = 21.5\ \text{mA}.$$

Minimal value of induction current:

$$I_{V(valley)} \quad \text{or} \quad I_V = 0.011\ \text{A} - \frac{21\ \text{m}}{2} = 0.5\ \text{mA}.$$

The conduction transistor losses accepting resistances $R_{ON-H} = 0.5$ Ohm for *IRF*540 and $R_{ON-L} = 40$ mOhm for *n*-channel *MOSFET IRF*540*N*:

$$P_{ON-H} = \left((0.011\ \text{A})^2 + \frac{(21.5\ \text{mA} + 0.5\ \text{mA})^2}{12} \right) \times$$

$$\times\ 0.5\ \text{Ohm} \cdot 0.5 = 4.03 \cdot 10^{-5}\ \text{W}.$$

$$P_{ON-L} = \left((0.011\ \text{A})^2 + \frac{(22\ \text{mA})^2}{12} \right) \times$$

$$\times\ 40\ \text{mOhm} \cdot \frac{6\ \text{V}}{12\ \text{V}} = 3.226 \cdot 10^{-6}\ \text{W}.$$

From the graphs in Fig. 4, the on-off time for a transistor with «high voltage» $t_{r-H} = 150$ ns (150 nanoseconds), $t_{f-H} = 0.25$ us (0.25 microseconds) and «low voltage» – $t_{r-L} = 0.90$ us, $t_{f-L} = 0.55$ us. Switching losses for the field-effect transistor *IRF*540 and *n*-channel *MOSFET*-transistor for the diode voltage $U_D = 1$ V in it, respectively, are equal to:

$$P_{SW-H} = \frac{1}{2} 12\ \text{V} \cdot 0.011\ \text{A} (150\ \text{ns} + 0.25\ \text{us}) 50\ \text{kHz},$$

$$P_{SW-L} = \frac{1}{2} 1\ \text{V} \cdot 0.011\ \text{A} (0.9\ \text{us} + 0.55\ \text{us}) 50\ \text{kHz},$$

$$P_{SW-H} = 1.32\ \text{mW}, \quad P_{SW-L} = 398.75\ \text{uW}.$$

According to graphic in picture 4, dead time loss, accepting dead time for rising $t_{Dr} = 275$ ns and dead time for falling $t_{Df} = 0.52$ us:

$$P_D = 1\ \text{V} \cdot 0.011\ \text{A} \times$$

$$\times\ (0.275\ \text{us} + 0.52\ \text{us}) \times$$

$$\times\ 50\ \text{kHz} = 0.4\ \text{mW}.$$

Reverse recovery loss in the body diode is calculated with the following equation:

$$P_{diode} = (0.275\ \text{us} + 0.52\ \text{us}) \times$$

$$\times\ 0.011\ \text{A} \cdot 1\ \text{V} \cdot 50\ \text{kHz} =$$

$$= 0.43725 \cdot 10^{-3} [W].$$

Capacitance loss in the *MOSFET* can be calculated with the following equation, where capacitance values are $C_{OSS-L} = 167\,pF$ for *IRF*540 and $C_{OSS-H} = 295\,pF$ for *IRF*540*N*:

$$P_{COSS} = \frac{1}{2} (167\ \text{pF} + 295\ \text{pF}) 12^2 \cdot 50\ \text{kHz} = 1.663\ \text{mW}.$$

The gate charge loss for transistors P_G, accepting voltage value for both high-side and low-side voltage transistors $U_{GS} = 0$:

$$P_G = (10\ \text{nC} + 5.4\ \text{nC}) 0 \cdot 50\ \text{kHz} = 0.$$

Operation loss caused by the control system – integrated circuit with a current consumption value $I_{CC} = 40$ uA: $P_{IC} = U_{in} I_{CC} = 12 \cdot 40\ \text{uA} = 0.48$ [uW].

The conduction loss in the inductor can be calculated more detailed from the graphic of inductor current. Discrete current resistance is equal to $DCR = 1.95$ Ohm.

$$P_{L(DCR)} = \left[(0.011\ \text{A})^2 + \frac{(21.5\ \text{mA} + 0.5\ \text{mA})^2}{12} \right] \cdot 1.95\ \text{Ohm},$$

$$P_{L(DCR)} = 161.3 \cdot 10^{-6} \cdot 1.95 [W] = 315.535 \cdot 10^{-6} [W].$$

Losses in the input and output capacitors $P_{CAP(ESR)} = I^2_{CAP(RMS)} \cdot ESR [W]$, accepting root mean square currents of the input and output capacitors are respectively equal:

$$I_{C_{in}(RMS)} = I_{out} \frac{\sqrt{(U_{in} - U_{out}) U_{out}}}{U_{in}} =$$

$$= 0.01\ \text{A} \frac{\sqrt{(12\ \text{V} - 6\ \text{V}) 6\ \text{V}}}{12\ \text{V}} = 5\ \text{mA},$$

$$P_{CAP(ESR)in} = (5\ \text{mA})^2 \cdot ESR,$$

$$P_{CAP(ESR)in} = (5\ \text{mA})^2 \cdot 0 = 0,$$

$$I_{C_{out}(RMS)} = \frac{\Delta I_L}{2\sqrt{3}} = \frac{20.3\ \text{mA}}{2\sqrt{3}} = 5.86\ \text{mA},$$

$$P_{CAP(ESR)out} = (5.86\ \text{mA})^2 \cdot ESR,$$

$$P_{CAP(ESR)out} = (5.86\ \text{mA})^2 \cdot 0 = 0.$$

ISSN 2664-9969

As a result, the total value of power loss and efficiency are equal:

$$P = P_{ON-H} + P_{ON-L} + P_{SW-H} + P_{SW-L} + P_{diode} + P_{COSS} + P_D + \\ + P_G + P_{IC} + P_{L(DCR)} + P_{C(in)} + P_{C(out)} = 0.005057 \text{ W},$$

$$P = 4.03 \cdot 10^{-5} + 3.226 \cdot 10^{-6} + 1.32 \cdot 10^{-3} + 398.75 \cdot 10^{-6} + \\ + 0.43725 \cdot 10^{-3} + 1.663 \cdot 10^{-3} + 0.4 \cdot 10^{-3} + 0 + 0.48 \cdot 10^{-6} + \\ + 315.535 \cdot 10^{-6} + 0 + 0 = 0.005057 \text{ W},$$

$$\eta = \frac{U_{out} I_{out}}{U_{out} I_{out} + P} = \frac{6 \text{ V} \cdot 0.011 \text{ A}}{0.066 \text{ W} + 0.004578 \text{ W}} \approx 93.5 \text{ \%}.$$

There are pictures in Fig. 7, which can describe impact of losses on the efficiency of buck voltage converter. There are diagram in Fig. 7, *a* and graphic of loss in Fig. 7, *b*. There are losses, which were received during the development of the electrical scheme of buck voltage converter.

Fig. 7, *a* shows the graphs of the dependence of the efficiency η on the active power $P_{out} = U_{out} I_{out}$. Analyzing graphs for constant values of power loss $P = 0.005057$ W, without capacitance loss in *MOSFET* and without taking into account without capacitance in *MOSFET* and «high-voltage» field-effect transistor losses.

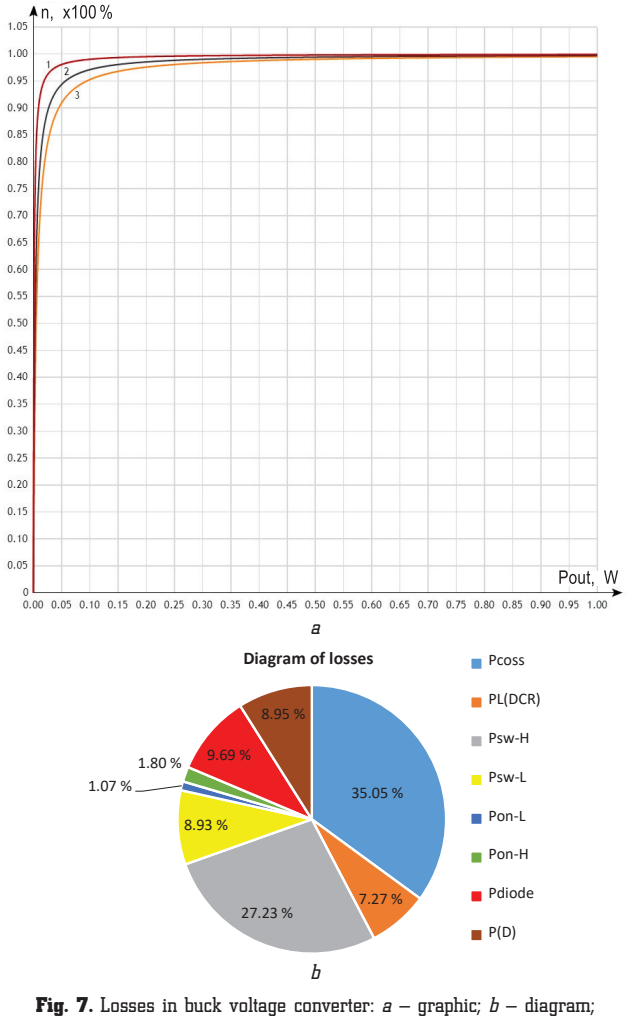


Fig. 7. Losses in buck voltage converter: *a* – graphic; *b* – diagram; 1 – all over the losses, 2 – without output capacitances of the «high-side» and «low-side» voltage level *MOSFET*, 3 – without output capacitances of the «high-side» and «low-side» voltage level *MOSFET*, switching-loss, reverse recovery loss in the body diode

Fig. 7, *b* shows a diagram of the power losses that occurred during the construction of the electrical circuit of the buck converter (Fig. 4). Thus, the largest value of losses falls on the output capacitances of the high-side and low-side *MOSFET* (35.05 %), switching-loss (36.16 %) and reverse recovery loss in the body diode (9.69 %).

4. Conclusions

The principles of technical implementation of a semiconductor buck voltage converter with a synchronous type of rectification, which can be used in wireless chargers, have been developed.

The possibility of creating a power supply based on the PWM of the DC input voltage is considered.

It is determined that for the practical implementation of a buck voltage converter based on an inductive-capacitive converter, it is advisable to use a digital control system. This scheme has been successfully tested, as evidenced by the relevant graphs.

The efficiency and loss power of the buck converter with synchronous rectification type are investigated, in particular, it is determined that the largest values of losses relate to the diode, the opening of the transistor gate and the capacitance of the output capacitor.

Synchronous rectification type of buck converters like this is widely used for specific loads. An enormous computer, increasingly power distribution architectures composed of power electronics are being considered or implemented for ships, cars, airplanes and so on. There are facilities to take advantage of alternative energy sources or attempt to increase efficiency and system availability.

References

1. Mulligan, M. D., Broach, B., Lee, T. H. (2005). A Constant-Frequency Method for Improving Light-Load Efficiency in Synchronous Buck Converters. *IEEE Power Electronics Letters, 3 (1)*, 24–29. doi: http://doi.org/10.1109/lpel.2005.845177
2. *Würth Elektronik Group, Electronic & Electromechanical Components «Switch Mode Power Supply Topologies Compared»*. Available at: https://www.we-online.com/web/en/electronic_components/news_pbs/blog_pbcm/blog_detail-worldofelectronics_45887.php
3. Ejury, J. (2013). *Buck Converter Design*. Infineon Technologies North America, 17.
4. *ROHM Semiconductor* (2016). Switching Regulator IC Series «Efficiency of Buck Converter», 15. Available at: www.rohm.com
5. Zheliazkov, Y. (2020). Circuit design of buck-voltage converter with digital control system. *Technology Audit and Production Reserves, 2 (1 (52))*, 46–50. doi: http://doi.org/10.15587/2706-5448.2020.202024
6. Schell, D., Castorena, J. (2007). Razrabotka ponizhaiuschego preobrazovatelia bez sekretov. *Komponenty i tekhnologi, 4*, 106–109.
7. *IR2184 High and Low Side MOSFET Driver*. Available at: https://www.hobbytronics.co.uk/ir2184-mosfet-driver
8. Chandran, N. K., Varghese, M. P. (2014). A New Control Strategy of Synchronous Buck Converter for Improved Light Load Efficiency. *International Journal of Science, Engineering and Technology Research, 3 (8)*, 2231–2238.
9. *PIC16F877A Microcontroller Introduction and Features*. Available at: https://microcontrollerslab.com/pic16f877a-introduction-features/
10. *PWM using Pic Microcontroller with Examples*. Available at: https://microcontrollerslab.com/pwm-using-pic16f877a-micro-controller/

Zheliazkov Yehor, *Department of Electronic Devices and Systems, National Technical University of Ukraine «Igor Sikorsky Kyiv Polytechnic Institute», Ukraine, e-mail: yehor.zheliazkov@i.ua, ORCID: http://orcid.org/0000-0002-3651-7840*