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**Volodymyr Ivakhno,
Volodymyr Zamaruiev,
Oleksandr Plakhtiy,
Volodymyr Nerubatskyi,
Maryna Filipieva**

CONSIDERATION OF DC/DC CONVERTER FOR PHOTOVOLTAICS WITH SOFT SWITCHING WITH MODIFIED PUSH-PULL CURRENT SOURCE INVERTER CIRCUIT

The object of research is the power part of the two-stage converter. The paper evaluates the parameters of the power part of the two-stage converter with transformer isolation, designed for the transfer of solar battery energy to the 400 V constant voltage network with the possibility of maintaining the maximum power point tracker (MPPT). The primary stage of the converter is made as a push-pull current source inverter topology with an additional switch, which is installed between the common point of the transformer's primary half-windings and the common point of the primary stage switches. The primary stage switches are made as a series connection of MOSFET transistors and Schottky diodes. The secondary stage has the traditional topology of a half-bridge voltage source inverter on MOSFET. A special switching algorithm of separated commutation is described, which provides non-dissipative snubber turn-on for of the current source inverter switches and their natural zero current turn-off switching (ZCS). The role of a snubber is performed by the leakage inductance of the transformer. For voltage source inverter switches, natural zero voltage switching (Zero Voltage Switching, ZVS) is provided. The role of non-dissipative capacitive switching snubbers may be performed by the MOSFET own output capacitance. The essence of this algorithm is to create a delay between the moment of forced switching on of the main key of the primary link and the moment of forced switching off of the transistor of the secondary link. There is also a small interval of energy return to the input source. Adjustment of the converter for the implementation of MPRT can be carried out by adjusting the ratio of the durations of the conduction state of the main and additional switches of the primary stage relative to the duration of the half-period of the frequency conversion. The types of switches were selected, static losses were estimated, simulation modeling was carried out in the MATLAB/Simulink environment, which confirmed the theoretical conclusions and the presence of soft switching modes.

Keywords: *photo energy systems, DC/DC converter, current source inverter, voltage source inverter, soft switching, MOSFET, Schottky diodes, static losses, MATLAB/Simulink.*

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1. Introduction

The general direction of world energy development is related to the wide use of renewable energy sources. This is due to the growth of demand for electricity with the simultaneous growth of efforts to eliminate emissions of common pollutants, decarbonization of electricity as a replacement for fossil fuels in transport, construction and industry. The dynamics of putting solar power plants into operation in recent years significantly exceeds this indicator for other sources of renewable energy, and this trend will continue. It is expected that in the European Union, the growth of rooftop solar photovoltaic units (SPU) will outpace the growth of large-scale power plants [1]. By custom, all SPUs are divided into residential, with a capacity of 3–11 kW, commercial – 100 kW–2 MW, and communal scale – 5–100 MW [2]. SPUs used in the residential sector, as a rule, have a storage battery as an intermediate energy storage device. Commercial and utility SPUs use separate battery energy storage systems (BESS). The difference in the structures of the SPU determines the different circuit solutions of the semiconductor energy converters used in the installations – these are hybrid converters with a DC/DC/AC structure with a constant voltage link and DC/AC converters with or without a built-in matching transformer [3–11]. In the European Union and some countries of the world, residential SPUs are limited to a capacity of 10 kW [12]. Existing converters allow the use of SPU as intended, but, as a rule, do not allow connecting low-power SPU in parallel to a common one,

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for example, with neighbors, BESS. Combining several SPUs with a constant voltage link allows to create an element of the MicroGrid structure, facilitates energy generation control, aligns the energy generation/consumption schedule, etc.

The work considers a direct current to direct current converter with galvanic separation of input and output links (DC/DC converter). This device can be powered by a solar panel with a maximum voltage of up to 50 V (the voltage at the point of maximum power is about 40 V) and a maximum power of 500 W and transfer energy to a receiver with a voltage of 400 V. This solution allows the use of low-voltage solar panels at the same time as a connection to a high-voltage BESS.

The energy efficiency of the converter is ensured by the use of the split switching algorithm [13–15], by simplifying the structural scheme of the SFU due to the exclusion of the dedicated maximum power point tracker (MPPT) unit with the transfer of this function to the converter under consideration. Split-switch converters (SSC) are DC/DC converters, i. e. two-link DC-to-DC converters with an intermediate high-frequency link and a transformer junction, and one of the links, for example, the primary, is built on the basis of a current inverter (CI), then secondary – voltage inverter (VI). The essence of the split switching algorithm is to create a delay between the moments of forced switching on of the power switches of the CI link and forced switching off of the keys of the VI link. As a result, as shown in a number of works with the participation of the authors (for example, papers [13–16]), turning off the controlled keys of the IC link is natural in the zero current switching (ZCS) mode, turning on the controlled keys of the VI link is also natural in zero voltage switching (ZVS) mode. The energy losses of turning on the CI keys can be significantly limited by means of inductive snubbers, which are connected in series with the keys and these snubbers are non-dissipative, and their role can be performed by the dissipation inductance of the transformer. The energy losses of turning off the VI keys can be significantly limited by means of capacitive snubbers, which are connected in parallel with the keys and these snubbers are also non-dissipative. That is, all switching of power switches (both on and off) can be soft (without the release of switching energy of a significant amount), and the limitation of switching losses can be such that their value can be neglected in comparison with static losses in the switches. Limiting switching losses allows to significantly increase the conversion frequency and, as a result, reduce the dimensions and mass of the reactive components of the converter (transformer, throttles, etc.). *The aim of the paper* is to estimate the amount of power losses in the power switches of the SSC (which is necessary to determine the efficiency). At the same time, the SSC is built according to a new scheme based on the zero topology of the CI link (zero scheme with an additional key), which should have a smaller value of the power of static losses of the keys in comparison with the known SSC scheme with a similar MPPT functionality based on the bridge topology of the CI link [16]. The purpose of simulation modeling is also to confirm the presence of soft switching of power switches in this new scheme.

2. Materials and Methods

Fig. 1 shows the SSC scheme, the idea of which was proposed in [13]. The converter consists of two links – primary and secondary, which are connected by an isolation transformer (Fig. 1), and the primary link is built on the CI basis, and the secondary – VI. The power switch of the CI link is built on the basis of a zero circuit with keys with reverse blocking ability based on *MOSFET* field transistors (transistors *VT*1, *VT*2 with diodes *VD*1, *VD*2 in series with the transistors, respectively) and an additional key based on transistor *VT*3 with a diode *VD*3 in series. The current source mode is provided by the throttle *L* connected to the input voltage source U_{in} and to the common point of the primary half-windings w_{1-1} and w_{1-2} of the transformer *T* (an additional switch *VT*3–*VD*3 is also connected to the same point). The switch IN is connected to the secondary winding w_2 of the transformer T according to the half-bridge scheme; VI power switches – *MOSFET* transistors *VT*4, *VT*5 with reverse diodes *VD*4, *VD*5, respectively, shunted by snubber capacitors *C*1, *C*2.

The converter operation algorithm is illustrated in Fig. 2, which shows the time diagrams of currents and voltages of the circuit under the assumption that the pulsations of the throttle current are insignificant, including the given control signals – voltages on the gates of transistors u_{GVT1}–u_{GVT5}. Voltages on transistors and keys *VS*1–*VS*3, which include transistors *VT*1–*VT*3 and diodes *VD*1–*VD*3 connected in series, on winding w_{1-1}, as well as currents of windings and transistors of the primary link are depicted.

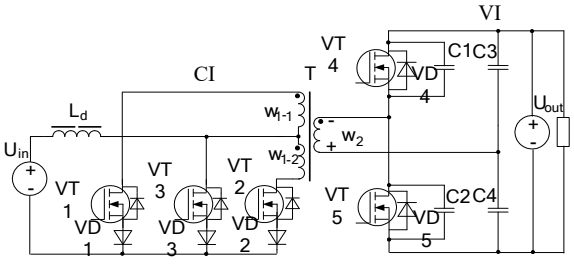

Fig. 1. Converter scheme

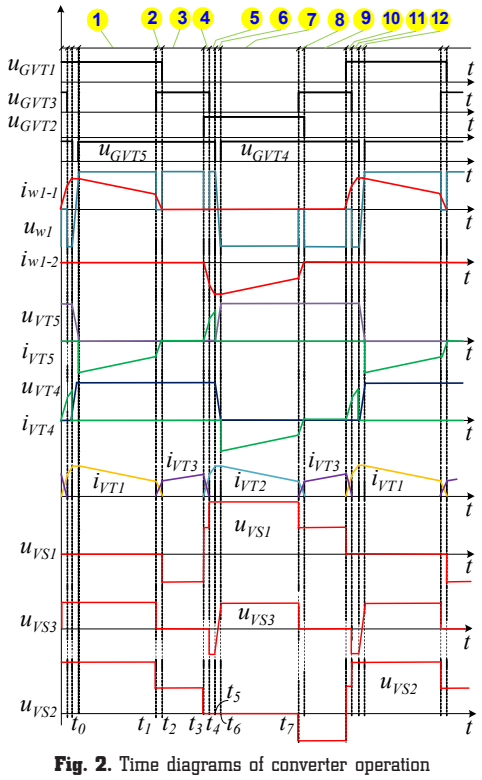

Fig. 2. Time diagrams of converter operation

The paths of current flow at the corresponding time intervals during the half-cycle of the converter are shown in Fig. 3. The operation of the circuit resembles the operation of the step-up converter circuit, i. e. the intervals of energy accumulation in the input throttle L_d and intervals of energy transfer to the load (to the output voltage source U_{out}) alternate. Next, let's consider the operation of the converter at intervals during the period of the conversion frequency (Fig. 2, 3). The ratio $U_{in}<(U'_{out})/2$ is fulfilled for the primary voltage source U_{in} and the load voltage U'_{out} reduced to the primary link.

t_0–t_1 – interval 1 of energy transfer to the load. Let the transistor *VT*1 be turned on, and the input current flows in the circuit of the throttle L_d – winding w_{1-1} of the transformer *T* (flowing from the beginning of the winding) – transistor *VT*1 – diode *VD*1, the current in the secondary circuit flows through the diode *VD*5 and the channel of the switched-on transistor *VT*5. The voltage $(U'_{out})/2$ *VT3* reduced to the primary winding of the transformer *T* is applied to the key *VT*3, and to the key *VT*2 – double, i. e. U'_{out}. At the end of the interval at time t_1, the transistor *VT*3 is turned on.

t_1–t_2 – interval 2 of the switching of the valves of the primary link. When the transistor *VT*3 is forcibly turned on, the current in the primary circuit also begins to flow through the switch *VT*3–*VD*3. The growth rate of this current is limited by the dissipation inductance of the transformer L_s (not shown in Fig. 2). And in the key *VT*1–*VD*1, the current decreases.

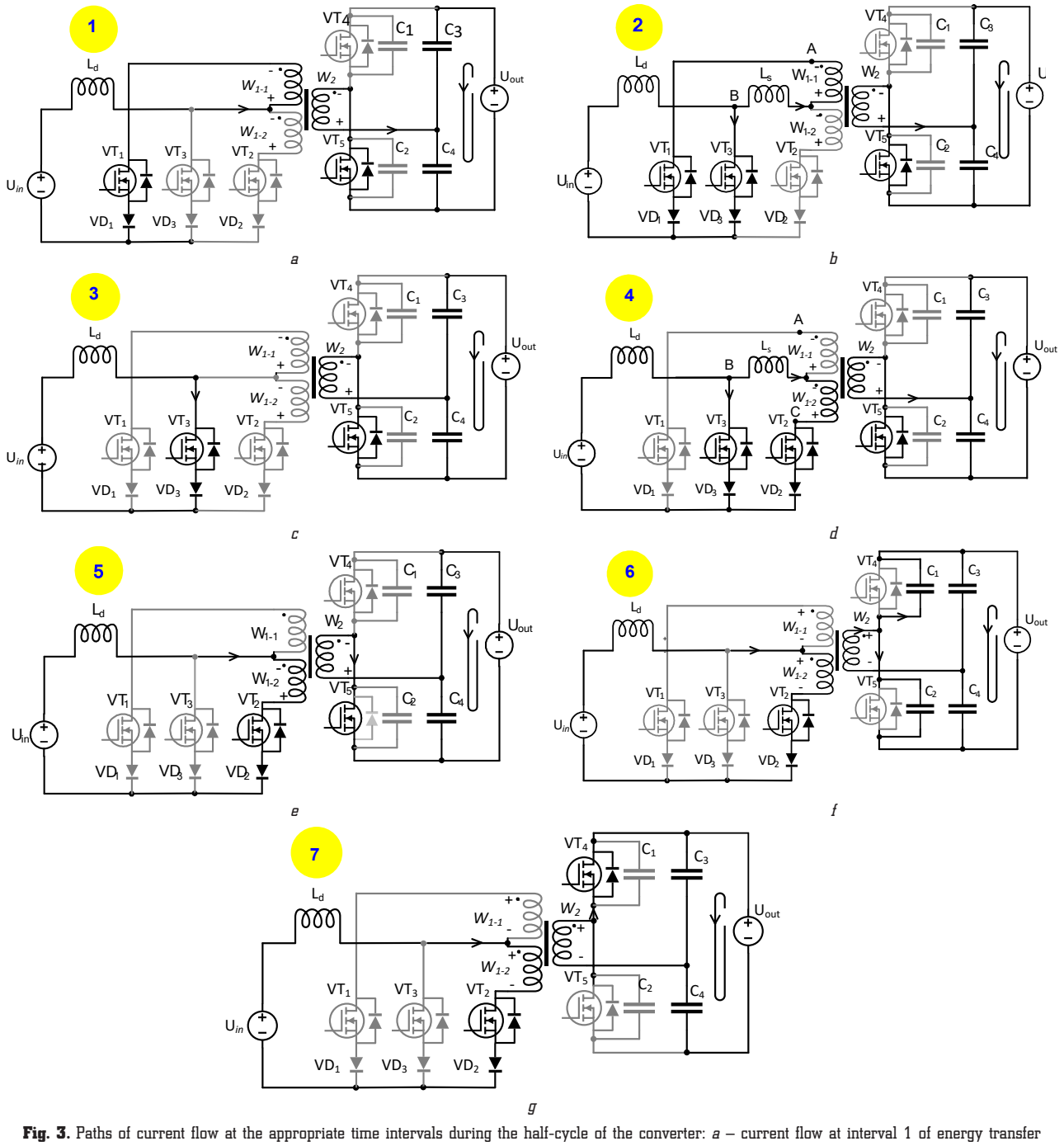

Fig. 3. Paths of current flow at the appropriate time intervals during the half-cycle of the converter: *a* – current flow at interval 1 of energy transfer to the load; *b* – current flow in interval 2 of switching valves of the primary link; *c* – current flow in interval 3 of energy accumulation in the throttle; *d* – current flow at interval 4 of switching valves of the primary link; *e* – current flow at interval 5 of returning energy to the power source; *f* – current flow at interval 6 of the snubber switch-off of the IN transistor; *g* – current flow at interval 7 of energy transfer to the load

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The inductance L_s acts as a snubber, limiting the switching losses of switching on the transistor *VT*3. The switching circuit of the keys consists of *VT*3–*VD*3, *VT*1–*VD*1, L_s, the voltage on the winding $w_{1\text{-}1}$, which is equal to $U'_{out}/2$. In this circuit, the voltage on L_s is compensated by the voltage $U'_{out}/2$, so the voltage on the physical winding w_{1-1} (between points A and B in Fig. 3, *b*) is zero. At the moment t_2, the current of the *VT*1–*VD*1 key, like the windings w_{1-1}, drops to zero, the *VD*1 diode receives a reverse voltage and turns off, that is, the *VT*1 transistor turns off naturally, in the ZVS mode. At the moment t_2, the transistor current drops to zero, or after a short period of time, the transistor can be turned off by the gate. At the end of interval 2, the throttle current, increasing, flows through the switch *VT*3–*VD*3 and interval 3 of energy accumulation in the throttle begins.

t_2–t_3 – interval 3 of energy accumulation in the throttle. At this interval, the throttle is connected by the *VT*3–*VD*3 key to the U_{in} source and its current increases, energy is stored. At the same time, there is no current in the primary windings, as well as in the secondary, and the voltage $U_{out}/2$ is applied to it, since the transistor *VT*5 is turned on. The voltage on *VT*1–*VD*1 is the inverse value of $U'_{out}/2$, and the voltage on *VT*2–*VD*2 is the same value. Interval 3 ends when transistor *VT*2 is turned on.

t_3–t_4 – interval 4 of the switching of the valves of the primary link. When the transistor *VT*2 is forcibly turned on, the current in the primary circuit also begins to flow through the switch *VT*2–*VD*2, the winding w_{1-2}, flowing into the beginning of the winding (at interval 1, the current flowed from the beginning, the rate of growth of this current is limited by the dissipation inductance of the transformer L_s, which in Fig. 1 is not shown), and the current decreases in the key *VT*3–*VD*3. The inductance Ls acts as a snubber, limiting the switching losses of switching on the transistor *VT*2. The switching circuit of the keys consists of *VT*3–*VD*3, *VT*2–*VD*2, L_s, the voltage on the winding w_{1-2}, which is equal to $U'_{out}/2$. In this circuit, the voltage on L_s is compensated by the voltage $U'_{out}/2$, so the voltage on the physical winding w_{1-2} (between points B and C in Fig. 3, *d*) is zero. At the moment t_4, the current of the *VT*3–*VD*3 key drops to zero, that is, the *VT*3 transistor turns off naturally, in the ZCS mode. At the moment t_4, the transistor current drops to zero or after a short period of time, the *VT*3 transistor can be turned off by the gate. At the end of interval 4, the winding current w_{1-2} flows into the beginning of the winding.

t_4–t_5 – interval 5 of energy return to the power source. At the beginning of interval 5, the *VT*2–*VD*2 switch is turned on and conducts the throttle current, the voltage on the *VT*3–*VD*3 switch is inverse by $U'_{out}/2$, and on the *VT*1–*VD*1 switch it is double direct, that is, U'_{out}. Since the transistor *VT*5 remains on through the gate and the voltage on the winding w_2 is fixed and has not changed, and the currents in the windings have changed their direction to the opposite, the direction of energy transfer has changed: energy is transferred from the source U_{out} to U_{in}, while the current of the transistor flows from the drain to the drain, and its diode does not conduct current. The circuit is in this state for a small part of the period.

t_5–t_6 – interval 7 of energy transfer to the load of the next half-cycle. In this interval and during the following intervals 8–10 of this half-period, the processes proceed similarly.

It can be seen that for the transistors of the primary link, snubber switching is carried out, while the switching snubber (dissipative inductance of the winding w_{1-1}) is non-dissipative, and the switching is natural ZCS, without losses. Transistor *VT*4 (*VT*5) is switched off by snubber, and the switch-off snubber (capacitors *C*1, *C*2) is non-dissipative, and the switch-on is natural ZVS, without losses. With the proper selection of snubber parameters, it is possible to ensure a sufficiently small value of switching losses, significantly smaller compared to static ones (as in resonant converters, but without the presence of a power oscillating circuit with a significant *Q* factor). It can also be seen that the flow time of the direct current of the transistor of the secondary link is insignificant, during the duration of the energy return interval 5.

The maximum direct voltage on transistors *VT*1, *VT*2 is U'_{out}, for transistor *VT*3 – $U'_{out}/2$, for diodes *VD*1–*VD*3 the reverse voltage is $U'_{out}/2$.

The output power is regulated by changing the ratio between the duration of intervals 1 and 3, so the MPPT option is available.

3. Results and Discussions

3.1. Evaluation of the main parameters of the converter. Let's make this assessment using the example of a converter which power source is a PNGNH60-B8 500W 182 solar panel [17]. The main parameters: nominal power P=500 W, voltage at the point of maximum power U_{in}=39.2 V, current at the point of maximum power I_d=12.75 A (nominal mode), open circuit voltage (no-load) U_{NL}=47.3 V, the output voltage of the converter U_{out}=400 V. Let's assume that the duration of the switching intervals 2, 4, 6 and the return interval 5 is small and it is possible to neglect their duration, as well as the pulsations of the throttle current and the output voltage U_{out}.

Let's specify the relative duration of the interval 1 τ_1 to the half-period $t_1=(t_1-t_0)/(t_6-t_0)$ for the idling mode at the level of t_1^{NL}=0.95, then the voltage U_{w1} on the primary winding should be $U_{w1}=U_{NL}/\tau_1^{NL}$=49.8 V. Since the voltage of the secondary winding U_{w2} is $U_{out}/2$=200 V, the value of transformation coefficient $K_T=w_2/w_1=(U_{out}/2)/U_{w1}$ will be 4.02. The forward voltage of switched-off transistors *VT*1, *VT*2 $U_{VT1,VT2}$ is equal to $U_{VT1,VT2}=2\cdot U_{w1}$=99.6 V, transistor *VT*3 – $U_{VT3}=U_{w1}$=49.8 V. The reverse voltage of diodes *VD*1–*VD*3 has the value $U_{VT1,VT2,VT3}=U_{w1}$=49.8 V.

For the nominal mode (maximum power mode), the relative duration of interval 1 τ_1^{nom} will be $\tau_1^{nom}=\tau_1^{NL}(U_{in}/U_{NL})$= =0.787, and interval 3 $\tau_3^{nom}=1-\tau_1^{nom}$=0.213. Then the value of the average current for the period of the keys *VT*1–*VD*1 and *VT*2–*VD*2 $I_{AV1,2}$ will be $I_{AV1,2}=I_d\cdot\tau_1^{nom}/2$=5.02 A, and the average current I_{AV3} of the key *VT*3–*VD*3 will be $I_{AV3}=I_d\cdot\tau_3^{nom}$=2.71 A.

As diodes *VD*1–*VD*3, let's take, for example, a Schottky diode of the VS-8TQ100-M3 type from Vishay Semiconductors [18] with nominal current $I_{F(AV)}^{nom}$=8 A and voltage V_R=100 V, for such a diode the voltage drop V_F at current $I_F=I_d$=12.75 A and the transition temperature T_j=125 °C is approximately V_F=0.62 V. Then the loss power $P_{VD1,2}$ for diodes *VD*1, *VD*2 will be according to $P_{VD1,2}=I_d\cdot V_F\cdot(\tau_1^{nom}/2)$=3.11 W for each, for diode *VD*3 – $P_{VD3}=I_d\cdot V_F\cdot(\tau_3^{nom})$=1.68 W, and for all diodes of the primary link $P_{VD1-3}=2\cdot P_{VD1,2}+P_{VD3}$=7.9 W.

As the transistors of the primary link, let's choose a transistor with a maximum drain-sink voltage of V_{DSS}=150 V (approximately one and a half times the margin) such that in the nominal mode the voltage drop on the switched-on transistor is approximately equal to the voltage V_F=0.62 V.

Then a transistor with a channel resistance is needed $R_{DS(on)}=V_F/I_d=0.049$ Ω (at the calculated junction temperature, for example, $T_j=100$ °C), for example, the SiR5710DP transistor from Vishay Semiconductors [19] with parameters: $V_{DSS}=150$ V, $R_{DS(on)}=0.0305$ Ω at $T_j=25$ °C and $R_{DS(on)}=0.051$ Ω at $T_j=100$ °C (all three CI transistors are the same). The voltage drop $u_{VT1(on)}$ on the switched-on transistor will be $u_{VT1(on)}=I_d\cdot R_{DS(on)}=0.65$ V, which will give the value $P_{VT1,2}$ of power loss $P_{VT1,2}=I_d\cdot u_{VT1(on)}\cdot(\tau_1^{nom}/2)=3.26$ W for each $VT1$, $VT2$ and transistor $P_{VT3}=I_d\cdot u_{VT3(on)}\cdot(\tau_3^{nom})=1.76$ W, and for all transistors of the primary link $P_{VT1-3}=2\cdot P_{VT1,2}+P_{VT3}=8.29$ W. The total static losses of P_{CI} in CI keys are $P_{CI}=P_{VD1-3}+P_{VT1-3}=16.2$ W, which is 3.2 % of the output power.

For transistors $VT4$, $VT5$, the voltage $U_{VT4,VT5}$ of the switched-off keys is U_{out}: $U_{VT4,VT5}=U_{out}=400$ V. Let's choose transistors with a limit voltage V_{DSS} in the range of 600–700 V. If the duration of switching intervals 2, 4, 6 and the return interval 5 are neglected it can be seen that the current flows through the reverse diodes. The amplitude of these currents I_{w2}: $I_{w2}=I_d/K_T=3.17$ A. The typical value of the voltage drop U_F of the built-in MOSFET diodes is 1 V: $U_F=1$ V. The required value of the $R_{DS(on)}$ channel resistance can be found based on the value of the drop on the switched-on transistor $u_{VT1(on)}=I_{w2}\cdot R_{DS(on)}=U_F=1$ V, then the value $R_{DS(on)}=u_{VT1(on)}/I_{w2}=0.32$ Ω is required at the transition temperature $T_j=100$ °C. Let's choose a SiHA180N60E transistor [20] with parameters: $V_{DSS}=650$ V, $R_{DS(on)}=0.18$ Ω at $T_j=25$ °C and $R_{DS(on)}=0.315$ Ω at $T_j=100$ °C, diode voltage U_F at current $I_{w2}=3.17$ A is 0.7 V. The average current IVDAV4.5 of the diode will be $I_{VDAV4,5}=I_{w2}\cdot\tau_1^{nom}/2=1.25$ A, power loss $P_{VD4,5}=I_{VDAV4,5}\cdot U_F=0.88$ W, in two transistors – $P_{VD4-5}=2\cdot P_{VD4,5}=1.8$ W. The power of P_{VI} losses in the P_{VI} keys will be the same: $P_{VI}=1.8$ W (0.35 % of the output power). Total losses in the keys of the converter $P_S=P_{CI}+P_{VI}=17.9$ W, which is 3.6 % of the output power. In a close solution, which is based on the same structure of the converter, which also provides modes of soft switching of the keys, but the CI switch is made according to the bridge scheme [16], the current of the primary winding flows through 4 keys – two diodes and two transistors. Including, during the intervals of energy transfer to the load and energy accumulation, therefore the total energy loss of the CI keys is doubled. Estimates of static losses carried out in [16] give the value of these losses at the level of 5.8 % of the output power, which is 1.6 times worse than in the considered converter.

3.2. Estimation of parameters of switching intervals. The duration of switching intervals 2 and 4 is affected by the value of the transformer leakage inductance L_s, which is reduced to the primary winding of the transformer. An estimate of its value can be given based on the value of the relative short-circuit voltage u_{sc}^* of the transformer $u_{sc}^*=\omega L_s/R_e$, where $\omega=2\pi f=3.14\cdot10^5$ s^{-1} is the circular frequency, $R_e=U_{in}/I_d=3.08$ Ohm is the equivalent load resistance of the transformer. Let's assume $u_{sc}^*=0.1$, then $L_s=u_{sc}^*/(\omega R_e)=1.04\cdot10^{-7}$ Hn. Duration of the interval $2\Delta t_2=(t_2-t_1)=(L_s\cdot I_d)/U_{w1}=25.7\cdot10^{-9}$ s. The total duration of intervals 2 and 4 will be $\Delta t_2+\Delta t_4=2\cdot\Delta t_2=53\cdot10^{-9}$ s, which is 0.5 % of the half-cycle duration and does not significantly affect the converter parameters.

The duration of the interval 6 of the snubber shutdown of the transistor $VT5$ is determined by the fall time of the transistor current t_f ($t_f=25\cdot10^{-9}$ s [20]), the switched current I_{w2} and the capacity of the snubber capacitors $C1$, $C2$. In the absence of a snubber, the switching energy E_0 is determined as follows [21]: $E_0=(U_{out}\cdot I_{w2}\cdot t_f)/2=10^{-5}$ J, and the switching loss power P_0 is $P_0=E_0\cdot f=0.8$ W. Installation of a snubber with a capacity of $C=(I_{w2}\cdot t_f)/(4\cdot U_{out})=50\cdot10^{-12}$ F ensures that the switch voltage reaches the voltage U_{out} at the moment t_f and reduces the energy and power losses of $P_{offVT4,5}$ by 6 times [12], to $P_{offVT4,5}=0.132$ W, that is, it makes it insignificant. According to the specification for the SiHA180N60E transistor, the latter has an output Coos capacitance of approximately 25 pF, and according to the variable component of the voltage, the capacitances of the two transistors are connected in parallel and the resulting capacitance is doubled, which makes it possible to exclude the installation of external snubber capacitors.

Thus, for this converter, there is no need for additional snubber components, their role is performed by dissipation inductance and output capacitances of transistors, and the influence of these components on the duration of energy transfer intervals is insignificant.

3.3. Simulation results. In order to check the theoretical provisions of the work, a simulation model of the proposed converter was created according to the scheme of Fig. 1 in the MATLAB/Simulink environment. The energy source is modeled by an array of photocells according to PNGNH60-B8 470-500W 182 data [17]. The parameters of the model correspond to the calculations of the above sections, and the control algorithms are shown in Fig. 2. The main purpose of the simulation is to confirm the soft switching of all converter keys.

The current and voltage oscillograms of the $VS1$ CI key are shown in Fig. 4. It can be seen that the key is turned off when the sign of the voltage on the key changes to negative, in the ZCS mode.

The current and voltage oscillograms of the $VT2$ CI transistor are shown in Fig. 5. It can be seen from the oscillograms that the transistor is turned on and off smoothly, at zero current or voltage.

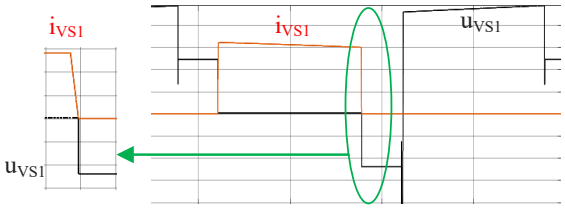

Fig. 4. Voltage and current of key $VS1$

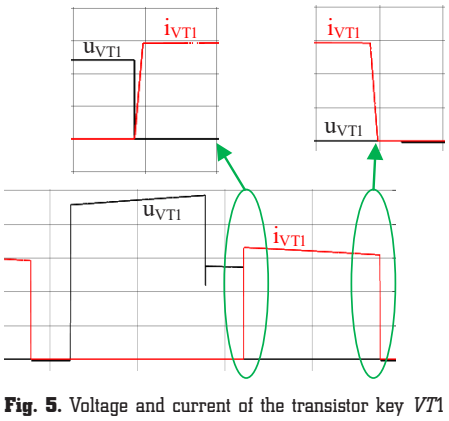

Fig. 5. Voltage and current of the transistor key $VT1$

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The oscillograms of the current and voltage of the *VT3* IC transistor, which provides a short circuit of the middle point of the transformer to the ground and the accumulation of energy in the throttle, are shown in Fig. 6. From the oscillograms, it can be seen that both forced switching on and switching off of the transistor occurs smoothly, at zero current or voltage.

The current and voltage oscillograms of the *VT4* VI transistor are shown in Fig. 7. It can be seen from the oscillograms that both the switching on (forced) and switching off of the transistor occurs smoothly, at zero current or voltage.

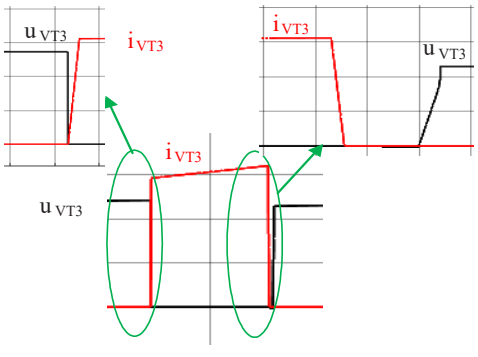

Fig. 6. Voltage and current of transistor *VT3*

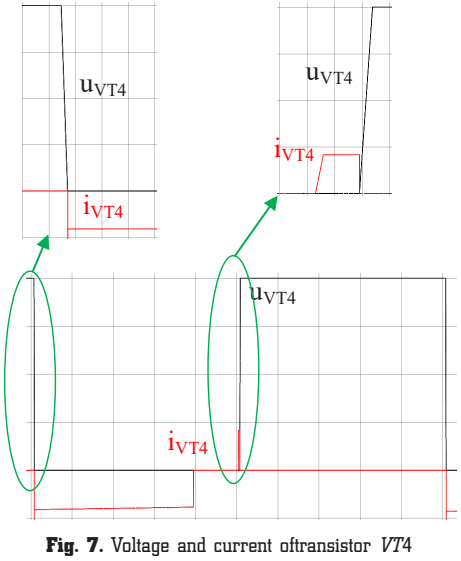

Fig. 7. Voltage and current oftransistor *VT4*

The simulation results shown in Fig. 4–7 fully correspond to the theoretically expected results from Fig. 2. The switching processes of all keys occur smoothly, which makes it possible to talk about the adequacy of the theoretical provisions and calculations presented in the work, since the model in the MATLAB/Simulink PowerSystem environment is built on their basis. The output power of the converter is close to 500 W, which confirms the correctness of the above calculations.

The practical significance of the obtained results is that the obtained schemes of semiconductor converters with separate switching and their proposed modes of operation allow the physical development of physical converters in solar energy systems with an improved efficiency exceeding 96 %.

The limitations of the presented study are the limitation of the power of the considered converter. When implementing the transmission of higher power, it is more appropriate to use full-bridge inverter circuits.

The scientific research was carried out in Ukraine during martial law, which significantly complicated its implementation, namely the conditions of power outages, air raids, damage to local infrastructure by enemy shells.

In further research on reducing the power losses and improving the efficiency of the converter with separate switching, it is advisable to analyze the possibility of applications of power transistors based on silicon carbide. It is urgent to carry out a physical simulation of the work of the converter in question to confirm the obtained theoretical principles. In addition, it is advisable to conduct a study of network inverters to analyze the process of transferring electrical energy from solar panels to alternating current electrical networks.

4. Conclusions

The work analyzes the processes in a two-link constant voltage converter with a conversion frequency of 50 kHz, designed to transmit the energy of a solar battery with a capacity of 500 W to a 400 V constant voltage network. The proposed topology of the primary link switch (CI based on a zero circuit with an additional key, keys – serial with connected MOSFETs and Schottky diodes) and secondary (traditional half-bridge VI on MOSFET) when using a special algorithm of synchronous control of keys – split switching algorithm – provide soft or natural switching of the converter keys. The selection of types of power switches was made and an estimate of the power of static losses was given (about 3.6 % of the original, which is 1.6 times better than the loss indicators of the switches of a similar solution with a bridge topology of the CI link). It was shown that in this case the role of non-dissipative snubbers can be performed by the dissipation inductance of the transformer and the output capacity of the MOSFET IN, and the total duration of the switching intervals is insignificant. Theoretical considerations regarding the nature of switching processes are confirmed by simulation modeling in the MATLAB/Simulink environment.

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Conflict of interest

The authors declare that they have no conflict of interest about this research, whether financial, personal, authorship or otherwise, that could affect the study and its results presented in this paper.

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Data availability

The manuscript has no associated data.

Use of artificial intelligence

The authors confirm that they did not use artificial intelligence technologies when creating the presented work.

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Volodymyr Ivakhno, *Doctor of Technical Sciences, Associate Professor, Professor of Department of Power and Biomedical Electronics, National Technical University «Kharkiv Polytechnic Institute», Kharkiv, Ukraine, ORCID: https://orcid.org/0000-0002-2122-6151*

Volodymyr Zamaruiev, *PhD, Associate Professor, Professor of Department of Power and Biomedical Electronics, National Technical University «Kharkiv Polytechnic Institute», Kharkiv, Ukraine, ORCID: https://orcid.org/0000-0003-0598-5673*

✉***Oleksandr Plakhtiy,*** *PhD, Associate Professor, Department of Electric Power Engineering, Electrical Engineering and Electromechanics, Ukrainian State University of Railway Transport, Kharkiv, Ukraine, e-mail: a.plakhtiy1989@gmail.com, ORCID: https://orcid.org/0000-0002-1535-8991*

Volodymyr Nerubatskyi, *PhD, Associate Professor, Department of Electric Power Engineering, Electrical Engineering and Electromechanics, Ukrainian State University of Railway Transport, Kharkiv, Ukraine, ORCID: https://orcid.org/0000-0002-4309-601X*

Maryna Filipieva, *PhD Student, Department of Electric Power Engineering, Electrical Engineering and Electromechanics, Ukrainian State University of Railway Transport, Kharkiv, Ukraine, ORCID: https://orcid.org/0000-0001-6499-7493*

✉*Corresponding author*